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Novel channel materials for Si based MOS devices: Ge, strained Si and hybrid crystal orientations

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Novel channel materials for Si based MOS devices: Ge, strained Si and hybrid crystal orientations

by

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Dedication

This work is dedicated to my parents, family and friends who have been a great source of encouragement and support.

Acknowledgements

First and foremost, I would like to express my gratitude to my supervisor, Dr. Banerjee for his utmost patience and encouragement, especially when things did not quite work out the way they were supposed to. He has been a great source of inspiration and his open-door policy has been my greatest asset during the course of my graduate studies. The support from the staff at the Microelectronics Research Center as well as SEMATECH / ATDF is greatly appreciated. It has been a great experience working with a wide range of collaborators from different fields and none of this work would have been possible without their efforts. My summer internships at IBM and ATDF / SEMATECH were great learning experiences and I appreciate all the inputs from the managers I worked with. Last but definitely not the least, all of this work would have been quite impossible without the enthusiastic support of my graduate student colleagues and friends. A lot of folks made significant contributions towards this endeavor and I will not try to list all of them, lest I omit anyone.

Novel channel materials for Si based MOS devices: Ge, strained Si and hybrid crystal orientations

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Integration of novel materials onto silicon substrates within a conventional CMOS framework is one of the most challenging problems facing the semiconductor industry. The evaluation of various novel channel materials such as Ge, strained Si and their alternative crystal orientations for high performance MOS devices is discussed. Techniques including the use of ultra-thin dislocation blocking layers for the epitaxial growth of Ge and strained Si, direct silicon bonding (DSB) for hybrid orientation technology (HOT) and surface passivation methods for Ge channel devices were explored in an effort to improve device performance while adhering to a CMOS-like processing scheme. Devices fabricated using low thermal budget processes with deposited high-k gate insulators and metal gate electrodes yielded significant mobility enhancements for strained Si NMOSFETs, hybrid crystal orientation devices, bulk Ge PMOSFETs as well as for PMOS devices fabricated on epi Ge layers grown on (110) Si substrates. Various tradeoffs were optimized to engineer the channel region as well as

source drain junctions for long channel MOSFETs. For the dislocation blocking layer technique, deep source drain implants to minimize junction leakage and an optimized strained Si layer resulted in 50% performance enhancement. In the case of DSB-HOT devices, optimized junction passivation utilized to reduce reverse diode leakage by an order of magnitude. This reduction, coupled with DSB layer thickness optimization, may enable the implementation of this technology at the 45 nm node and beyond. The electrical quality of the bond interface for DSB wafers was also evaluated. An asymmetry in the forward and reverse current voltage characteristics was observed in spite of an oxide free bond interface. This asymmetry was attributed to a new type of junction formed at the (110) / (100) Si bond interface due to a valence band offset between the two different Si surfaces. Consistent with the experimental observation, density functional theory simulations also predict the existence of such a band offset. For bulk Ge devices, a thin SiO_X interfacial layer was utilized to passivate the Ge / high-k interface and demonstrate a 2X enhancement over universal Si / SiO_2 hole mobility.

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Chapter 1: Introduction

Conventional Complementary Metal Oxide Semiconductor (CMOS) technology is moving very close to the physical limits of the geometric scaling paradigm pursued by the semiconductor industry for the last 40 years or so. Improvements to the design of highly scaled devices have almost ceased to provide the power, performance and Si real estate benefits that were seen in the past. This therefore, makes it a very exciting juncture in terms of research and development and various alternative materials are being explored to enable the continued exponential improvements in performance, power and functionality. From a front-end CMOS device perspective, these new materials can be divided into four technology elements – the semiconducting material which forms the channel, the gate insulator, the gate electrode itself and the junctions. Each of these elements has been the focus of extensive research over the last decade as the benefits of geometric scaling have reduced significantly.

Strain, both biaxial as well as uniaxial, has been one of the most interesting means of modifying the electronic band structure of the channel material which can be attained with little change to the basic Si / SiO_2 gate dielectric technology. Various techniques have been proposed to incorporate strain in the channel. From a product perspective, the most successful among these have been the introduction of SiGe in the source drain regions[1], the use of tensile and compressive liners [2,3] as well as the stress memorization technique[4]. In the initial stages of the research on strained material systems, biaxially strained layers of Si[5] and Ge[6] have also served as very interesting research tools for the

evaluation of the impact of strain on carrier mobility. It is envisioned that the right combination of global biaxial and local uniaxial strain could be used concomitantly to provide additional improvements to the low field mobility. It has also been argued that the enhancement in low field mobility does in fact translate to a significant, but not equivalent, improvement in the source injection efficiency for highly scaled devices[7]. For a MOSFET channel, the carriers are confined to a roughly triangular potential well. As a result of this, the energy levels available to the carriers are quantized and the valley degeneracy is lifted. Fischetti *et al.*[8] argued that the band splitting due to confinement is much more significant than the band splitting due to strain. Hence, the significant enhancements seen in carrier mobility may not be entirely attributed to the reduction in scattering probability due to band splitting – a very similar splitting exists in unstrained materials in MOSFETs as well. From their simulation results, it was argued that a significant reduction in surface roughness scattering would be necessary to explain the observed enhancements in mobility. To some degree, the improvement in drive current and performance would then be accompanied by an increase in the offstate leakage for most of these technologies.

The focus of this dissertation is the evaluation of some of the technological alternatives for the integration of channel materials such as Ge and strained Si into a simple MOSFET process flow using MOS devices fabricated on both conventional and alternative orientations of the surfaces of these materials. Replacing the channel material is a very significant change from a manufacturing standpoint and such a modification has not successfully made it into volume production for conventional CMOS logic

technology. A channel material change would probably be appropriate for technology nodes much further down the International Technology Roadmap for Semiconductors (ITRS) [9] scaling roadmap after the introduction of both high-k metal gates and fully-depleted devices using Si channels such as Fully Depleted Silicon On Insulator (FDSOI) and multiple gate FINFETs in their various embodiments have been demonstrated in a manufacturing scenario. At the same time, in order for alternative channel materials to be viable candidates for incorporation into a product, they would likely be used in some form of fully depleted material-on-insulator configuration probably initially for niche, very high performance applications. The development of alternative growth techniques for the deposition of good quality Ge and strained Si without the growth of thick relaxed SiGe buffer layers is very attractive from a cost standpoint and such techniques would hopefully make these materials more easily accessible for products that are targeted at a more cost sensitive market. Other materials, notably III-V semiconductors currently are a very hot area of research for high drive current CMOS applications. Back-of-the-envelope calculations of the products of bulk carrier mobility and available effective density of states (N_C, N_V) for a few different materials for both electrons and holes are plotted in Fig. 1.1 This product is an interesting quantity for a very preliminary comparison of candidate materials since it indirectly compares the maximum possible carrier speed and highest possible carrier density that may be achieved for each of the materials considered. Germanium, for holes, shows a significant improvement over all the other materials considered in Fig. 1.1.

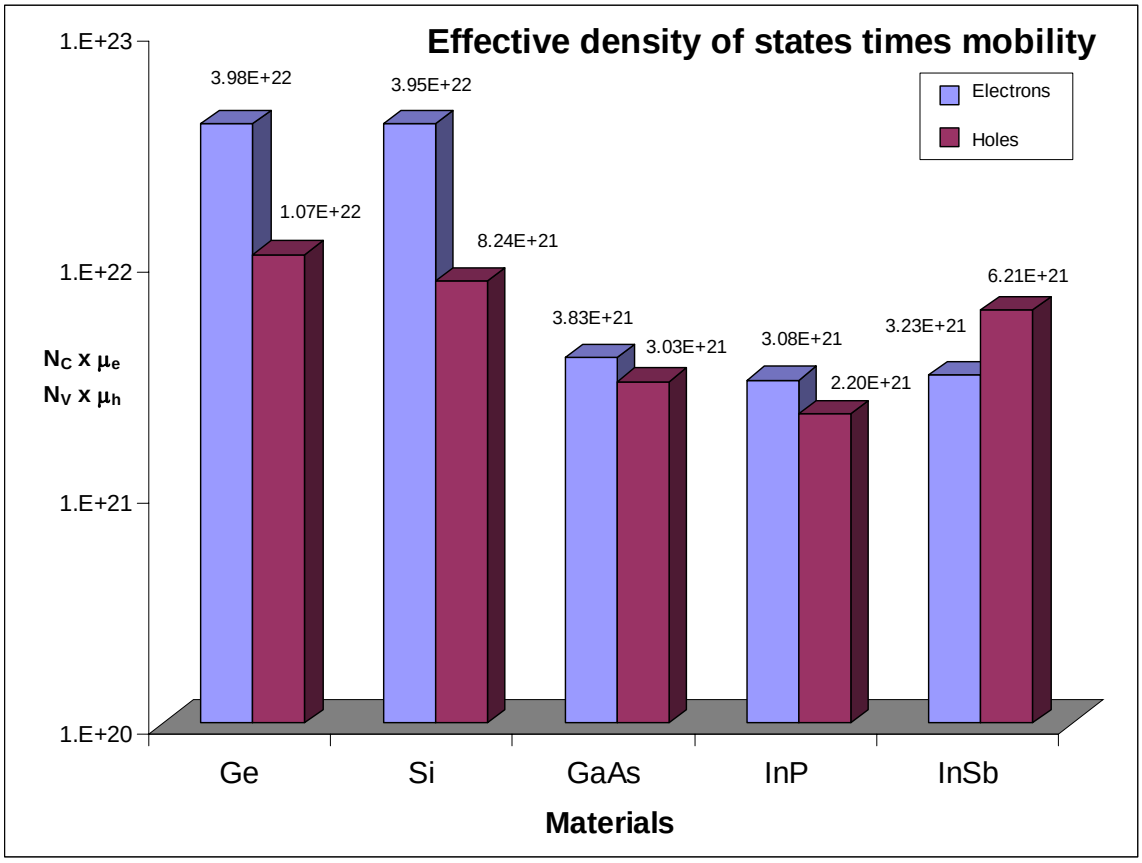


Fig 1.1: A comparison of the product of effective density of conduction and valence band states and bulk unstrained mobility of various materials suggests about 30% improvement for Ge PMOSFETs over Si. III-V materials and Ge for NMOSFETs may not be promising.

The situation for electrons is a bit disappointing. III-V materials come up about an order of magnitude lower for both electrons and holes, primarily because of a much lower available density of states, even though carrier mobility is much higher. Such a comparison must be used cautiously. For instance, band gaps were not considered in this comparison – the band gap of Ge is 0.66 eV, about half of Si (1.12 eV) which would

inherently mean higher off state leakage and a worse I_{ON}/I_{OFF} performance. In comparison, the bandgap of GaAs is 1.43 eV. Also, interface preparation for Si is much better optimized than for any of the other materials and in current high performance devices, mobility is usually limited by surface roughness scattering.

1.1 $Si_{1-X}Ge_X$ DISLOCATION BLOCKING LAYERS

Chapter 2 discusses the evaluation of alternative growth techniques to obtain good quality Ge layers by leveraging the idea of dislocation blocking due to strain fields. MOS capacitors, diodes and MOSFETs were fabricated for this purpose. Some promising results have been obtained by the use of a dislocation blocking layer stack comprising of multiple SiGe layers. This stack was used to obtain both strained Si and Ge films on Si substrates without the growth of several microns of a buffer layer[10,11]. This demonstration was also leveraged in other collaborative research to grow GaAs on a Si substrate using the Ge on Si layers as a starting material[12]. For practical applications, once the layers of interest have been grown on regular Si handler wafers, it is envisioned that the topmost layer would be used in a semiconductor-on-insulator structure while the dislocation blocking layer stack on the Si handler wafer may potentially be reused for the epitaxial growth of more material. This way, the defects in the dislocation blocking layers are entirely eliminated from the actual device region. Recess etching and selective deposition of lattice mismatched source drain regions to additively couple uniaxial / biaxial tensile or compressive strain into the Ge or III-V channels is the next obvious way of scaling this material system further. For instance, selective Si or SiGe epitaxy in the

source drain areas of a relaxed Ge on insulator device would lead to uniaxially tensile strained Ge.

1.2 INTERFACE ENGINEERING FOR DEPOSITED GATE INSULATORS

In order to ameliorate short channel behavior as we continue the geometric scaling trend, the gate insulator thickness has been scaled continuously almost to the point where gate leakage constitutes a significant component of the off state leakage of the device. In cutting edge high performance products, heavily nitrided oxides of silicon with thicknesses of about 1 nm are being used now. This constitutes a few mono-layers of insulating material between the channel and the gate electrode. This raises a lot of concerns about both leakage power consumption as well as reliability. One obvious way to minimize gate leakage while maintaining effective gate control on a short channel devices is to increase the permittivity of the gate insulator by the use of high-k materials. Typically, most high k materials are deposited, though some other interesting ones may be grown epitaxially[13]. The progress of such deposited gate insulators on Si has been a major driving force behind revisiting other channel materials such as Ge and GaAs – since the native oxides of these materials do not possess the high quality of the Si / SiO_2 system, one of the more promising ways to achieve well passivated interfaces for alternative channel materials is to utilize deposited insulators with modified interfacial treatment to passivate the interface. Epitaxial insulator growth is another approach but involves the added complexity of lattice matching. For ultra thin insulators, this may well become more and more interesting. An engineered gate insulator, probably with multiple layers to serve different needs is currently the leading candidate to solve this problem.

For high k / metal gate stacks on Si substrates – this would constitute a thin SiO_X interfacial layer that provides a high quality interface and a slightly thicker high-k layer on top of this that reduces leakage and improves the gate control. A similar philosophy of using a bi-layer stack of a high band gap material to passivate the interface and a thicker over-layer with larger permittivity and consequently a lower band gap is an interesting path to enable surface channel MOS devices with new channel materials such as Ge and III-V materials. In chapter 3, experiments using bulk Ge substrates to optimize the interface between Ge and high k gate dielectrics are described. HfSiO[14] which has shown the most promising results on bulk Si substrates was the primary focus of this work which primarily focused on interfacial layer engineering including the deposition of an ultra-thin SiO_X interfacial layer on Ge substrates for the fabrication of MOSFETs with high k / metal gate stacks. This yielded a significant enhancement in the hole mobility of about 2X the universal Si / SiO_2 hole mobility and a peak mobility of 332 cm^2/V-s.[15]

1.3 DIRECT SILICON BONDING FOR HYBRID ORIENTATION TECHNOLOGY

Another attractive way of enhancing channel mobility without the introduction of any new channel materials is the use of hybrid crystal orientations of Si substrates. A 2 – 3 X boost in hole mobility and about 40 – 60% improvement in I_{ON}/I_{OFF} performance for PMOS devices is possible by merely changing the starting crystal surface to a (110) Si instead of the typically used (100) Si. However, if the same surface is used for NMOSFETs, a degradation of similar magnitude in the electron mobility is observed. Various techniques have been proposed to utilize the (100) Si for NMOS and (110) Si for PMOS devices in a silicon-on-insulator configuration[16] as well as a bulk-like technology

achieved by Direct Silicon Bonding (DSB)[17]. In chapter 4, as part of the research on novel channel materials, experimental work on DSB wafers is discussed. One set of experiments targeted the electrical evaluation of the quality of this bond interface by the fabrication of vertical resistor structures to study the impact on electrical conductivity. A novel physical phenomenon – the existence of a band offset between two layers of Si with differing crystal orientations – was observed from these experiments. Collaborative work was done using Density Functional Theory (DFT) to calculate a band offset value of about 85 meV between the valence bands. This was further utilized in a conventional device simulator to confirm the same qualitative behavior. Even though ultra-thin DSB layers are attractive from a Shallow Trench Isolation (STI) scaling standpoint, if the bond interface is very close to the device, high leakage is observed. In order to reduce the thermally-assisted junction leakage due to the dangling bonds at the bond interface in the depletion region, junction passivation by the use of F, N and H_2 implants was studied.

1.4 HYBRID CRYSTAL ORIENTATIONS FOR EPITAXIAL Ge ON Si

Chapter 5 describes the final set of experiments that integrate the work on the dislocation blocking technique for growth on Si, interface engineering for Ge and the added advantages offered by the alternative crystal orientation for hole mobility. Germanium layers grown on a (110) Si substrate using the dislocation blocking have also shown significant enhancements in the hole mobility as compared to both universal Si (100) and measured data from bulk Si (110) and bulk Ge (100) as the channel materials. Electrical data on these MOSFETs is presented, along with some initial material characterization. Further material characterization is suggested as part of the future work

to optimize epitaxial growth quality on (110) Si surfaces and achieve smooth pure Ge epi layers on other crystal orientation surfaces.

1.5 SUMMARY AND FUTURE DIRECTIONS

Chapter 6 is a summary of the highlights of the research and experiments described in the prior chapters. We comment on the broader aspects of all experiments on novel channel materials. Relative merits of various candidate materials for high performance devices need critical evaluation. For instance as part of this work, both Ge and hybrid crystal orientation Si were studied and the benefits for PMOS devices are very similar – in such a scenario, the adoption of a Si based technology would probably be much more appealing. The use of Ge, however, holds the promise of additional strain engineering and need not be exclusive of the hybrid orientation advantages as shown in the final experiment. As we proceed further along the ITRS roadmap, other considerations such as lower power consumption, integration of mixed functionality on a single chip and lower costs, apart from improvements in performance would become more and more critical, depending upon the targeted niche applications of such advanced technologies.

Chapter 2: Dislocation blocking layer templates for lattice engineered strained Si and Ge channel devices

2.1 MOTIVATION

Channel engineering has emerged as one of the most aggressively pursued areas for dramatically improving CMOS performance[18,19]. In particular, tensile-strained Si for NMOS[1] and Ge for PMOS[2] have attracted researchers' attention. Biaxially tensile strained Si has been shown to exhibit significant mobility enhancements (~1.8 – 2X) over bulk Si NMOS devices[1]. Bulk Ge has ~4.2 X improvement in the hole mobility over Si. Either of these materials could enable CMOS performance improvements for future technology generations. Significant technological challenges still remain before these can be implemented in a manufacturing scenario. Biaxially tensile strained Si NMOS technology is constrained by the process complexities and cost of growth and chemical mechanical polishing for the 1 – 2 μm thick relaxed SiGe virtual substrates. High hole mobility has been achieved on bulk Ge substrates for PMOS devices[20], but these are too expensive and fragile to be manufacturable. They are more suitable for interface engineering experiments where a high quality wafer is very important as will be discussed in chapter 3. Germanium grown directly on Si substrates has received significant attention recently. Nayfeh *et al.*[21] reported on the growth of ~ 400 nm thick Ge layers with a surface roughness of ~2.9 nm for PMOS devices.

This chapter discusses a technique of growing strained-Si and relaxed-Ge channels on Si substrates using an ultra-thin (~ 100 - 150 nm) $Si_{1-x}Ge_x$ dislocation blocking layer with rapid but distinct step changes in the Ge mole fraction. This avoids the complexity and cost of thick epitaxial growth[22,23] and chemical mechanical polishing[24,25]. Other, more complex methods such as Molecular Beam Epitaxy (MBE), He implantation[26] and C incorporation at interfaces during growth[27] have been reported for the growth of significantly thin buffer layers. The technique described here creates multiple $Si_{1-x}Ge_x$ interfaces within the buffer layer. Large strain fields are present at these interfaces which help terminate the threading dislocations into loops by an interface blocking mechanism[28,29]. As a result, smooth films of both strained Si and Ge were obtained on Si substrates by using multiple, thin (100 – 200 nm) $Si_{1-x}Ge_x$ layers.

2.2 MATERIAL GROWTH AND CHARACTERIZATION

The film growths were carried out in an UHVCVD system on (100) Si wafers using disilane and germane as the Si and Ge precursors. Partially strained $Si_{1-x}Ge_x$ layers are grown on the Si substrate followed by a pure Ge layer. The Ge concentration in the SiGe layers was varied rapidly resulting in three layers of $Si_{1-x}Ge_x$ with x=0.2, x=0.25 and x=0.4 respectively. The growth temperature for the first two layers were 440°C and was subsequently lowered to 400°C for the 40% Ge layer. Following the partially compressively strained SiGe graded layers a pure Ge layer was grown at a temperature of ~400°C. For comparison a pure Ge layer at the same condition was also grown *directly* on the Si substrate. Material characterization of the pure Ge layer was done using atomic force microscopy (AFM) to determine the surface roughness, transmission electron

microscopy (TEM) to determine the location of dislocations and other possible defects, X-ray diffraction(XRD) and secondary ion mass spectrometry (SIMS) for determining the layer compositions, and Raman spectroscopy to determine the strain in the layers. SIMS measurements for the Ge sample grown with three $Si_{1-x}Ge_x$ layers of different Ge mole fraction between Si substrate and the Ge layer, showing the Ge concentration vs depth is shown in Fig 2.1.

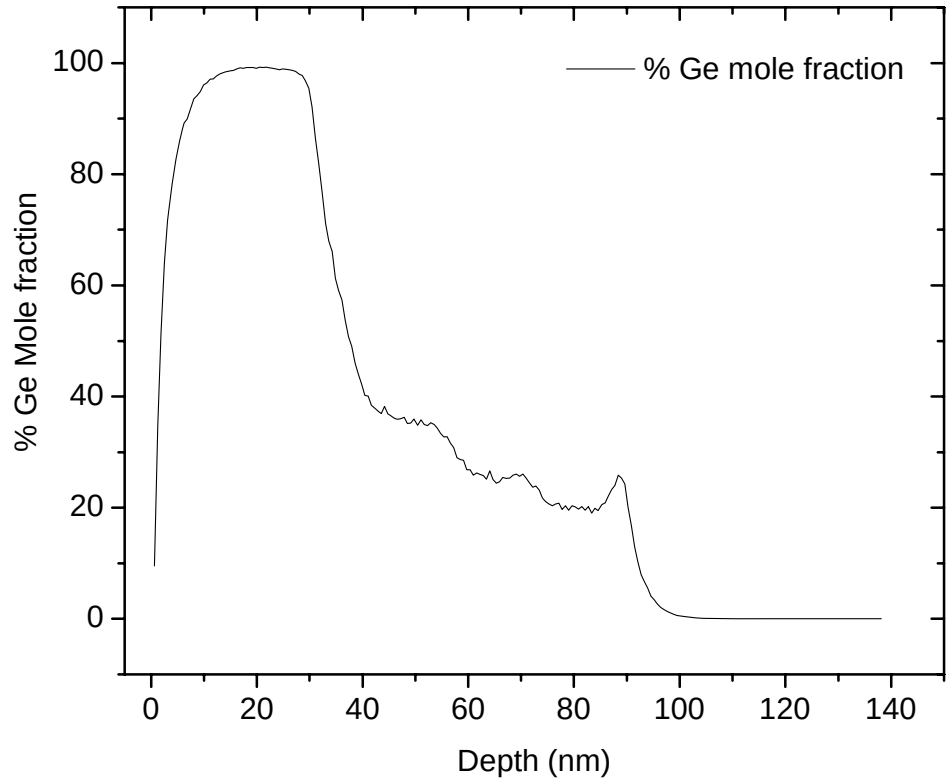


Fig 2.1 SIMS results for Ge grown on Si substrates using the dislocation blocking layer technique indicate a rapid, distinct change in mole fraction, which results in large strain fields at the interfaces and effectively blocks dislocations from threading towards the surface.

The Ge layer has a thickness of ~30nm. The total stack height was ~90nm which is much thinner than typically fully relaxed SiGe buffer layers. Fig 2.2 is a Z-contrast TEM image of the sample which also shows the interfaces with varying Ge concentration.

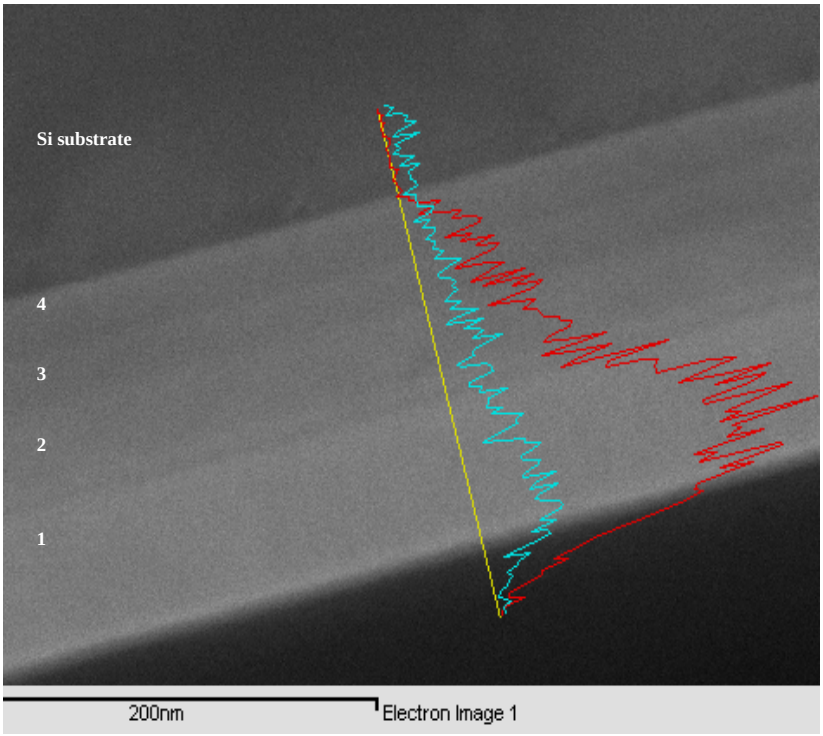


Fig. 2.2 Low magnification TEM imaging illustrates the sudden change in the mole fraction as a change in the image contrast where different SiGe interfaces are clearly observed. An EDS linescan (red line) show the Ge mole fraction.

An Energy Dispersive Spectroscopy (EDS) line scan is also presented in Fig 2.2 that shows a high Ge concentration in the top layer which subsequently decreases with depth. This is quite different from the Ge on relaxed graded SiGe buffer layer growth

technique where the graded SiGe is much thicker (1-2μm), requiring more complex growth techniques.

Surface roughness of the films grown was characterized using AFM and the above-mentioned sample with Ge on three strained $Si_{1-x}Ge_x$ layers was found to have a RMS surface roughness of 0.51nm as shown in Fig. 2.3.

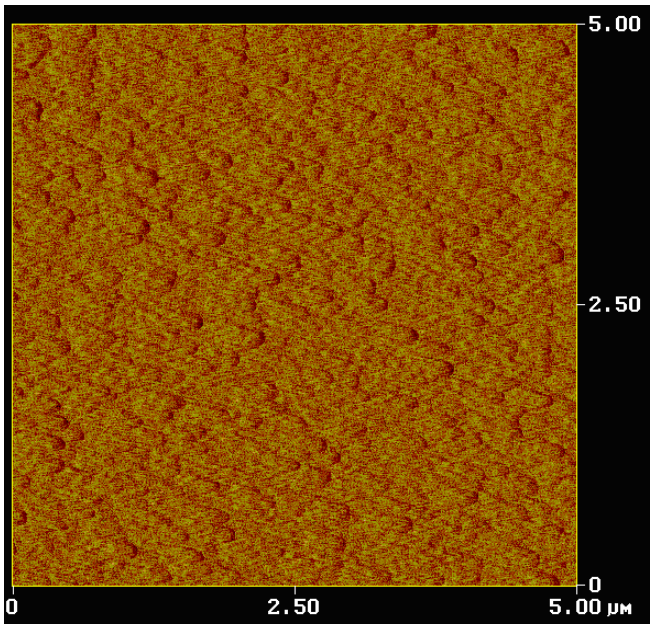


Fig. 2.3 AFM imaging shows a RMS surface roughness of 0.51 nm which is comparable to that observed on bulk Si substrates

The smoothness of the Ge film was seen to degrade as the number of SiGe layers between the Ge and the Si substrate was decreased and was found to be worst when Ge is grown directly on Si (RMS roughness of 1nm) as shown in Fig 2.5.

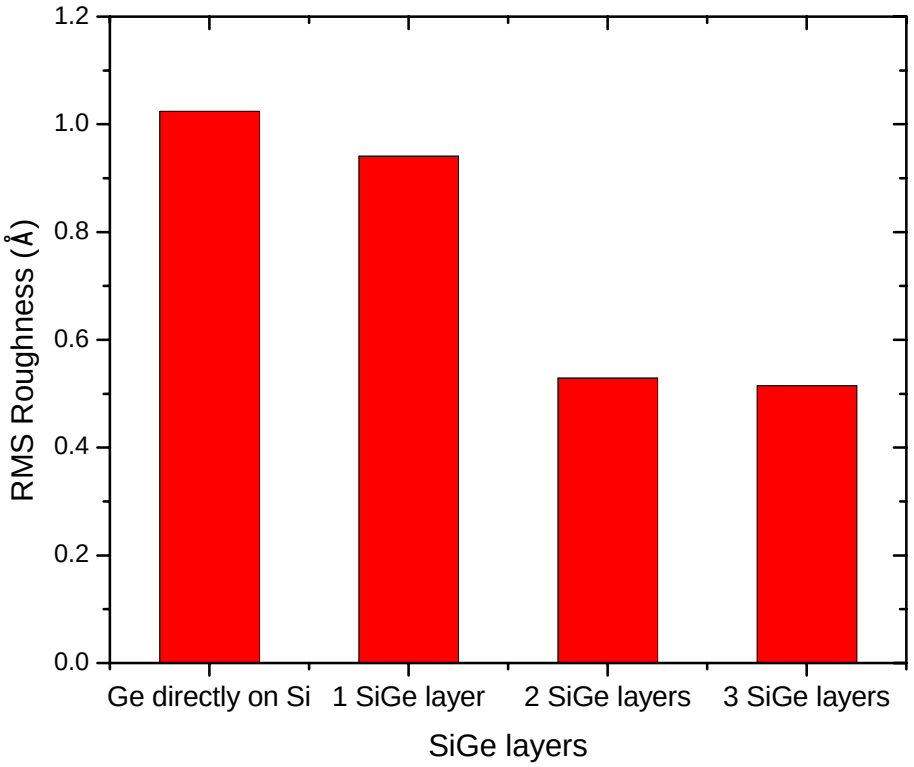


Fig. 2.5 RMS surface roughness plotted as a function of the number of SiGe dislocation blocking layers illustrates a significant increase for epi Ge grown directly on Si substrates.

The Ge layer grown directly on Si is the most defective and the roughest because of the large (4%) lattice mismatch. It is believed that the growth mode becomes more planar as the $Si_{1-x}Ge_x$/ $Si_{1-y}Ge_y$ interfaces are introduced. Cross-sectional TEM images show this behavior in Fig 2.6. The defects are blocked at the $Si_{1-X}Ge_X$ interfaces. Most of the defects are located in the $Ge/Si_{0.6}Ge_{0.4}$ interface. In this interface the presence of elastic deformation (strain fields) due to the mismatch of the lattice parameter between the two

layers is observed. Some dislocations and stacking faults can be seen at the other interfaces.

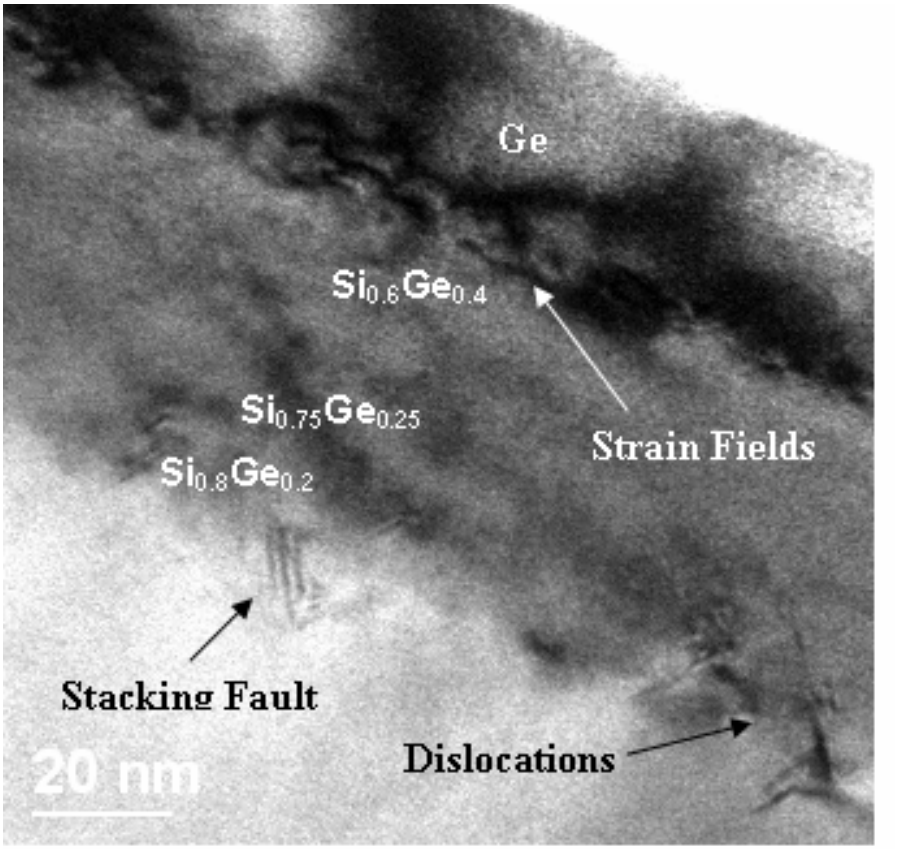


Fig. 2.6 Low magnification TEM images illustrating the multi-layer $Si_{1-x}Ge_x$ stack and the formation of dislocations in the lower portion of the stack.

A defect-free high quality Ge layer on top was observed in the higher magnification image shown in Fig 2.7. The presence of these strain fields indicates that the interface blocking mechanism might be due to the dislocation bending due to these strain fields. Under the strong strain fields present at the $Ge/Si_{0.6}Ge_{0.4}$ interface the

dislocations bend and probably move along the interface or form localized dislocation loops leading to effective blocking of the dislocations at this interface.

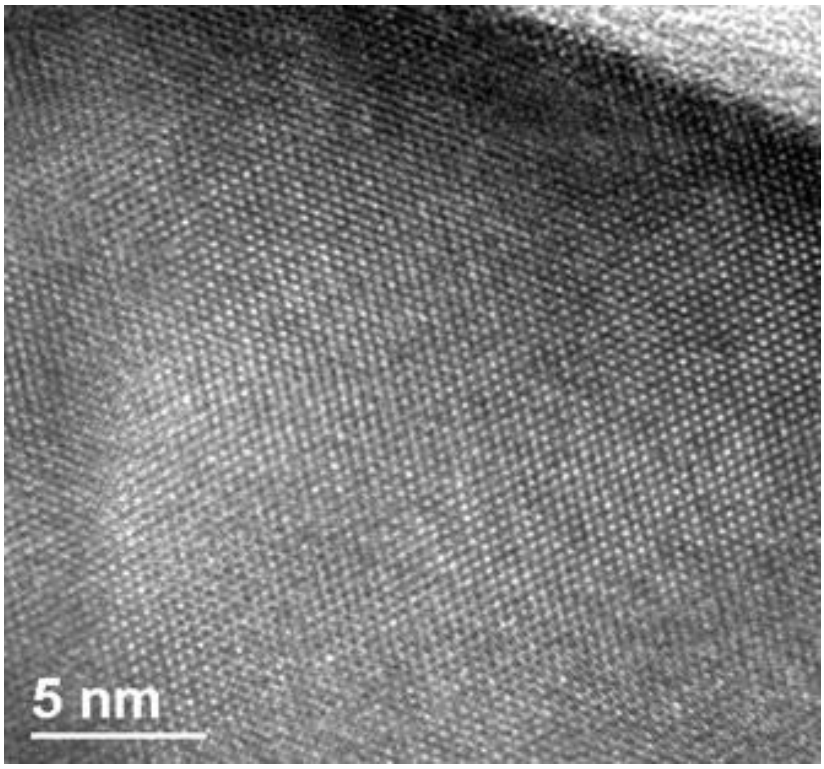


Fig 2.7 High magnification TEM images of the top Ge layer shows single crystal Ge epitaxial growth. However, statistically significant etch pit density data is required to support the claim of dislocation blocking.

To further analyze the defects in the film high resolution plan-view TEMs (Fig 2.8) were also prepared. Although the sample preparation for the plan-view TEM and polishing led to non-uniformity and damage of the sample it revealed the ordered crystal plane alignments and a regular cross hatch morphology which is typically considered to

be an indicator of good material quality for the Ge grown on the dislocation blocking layer template.

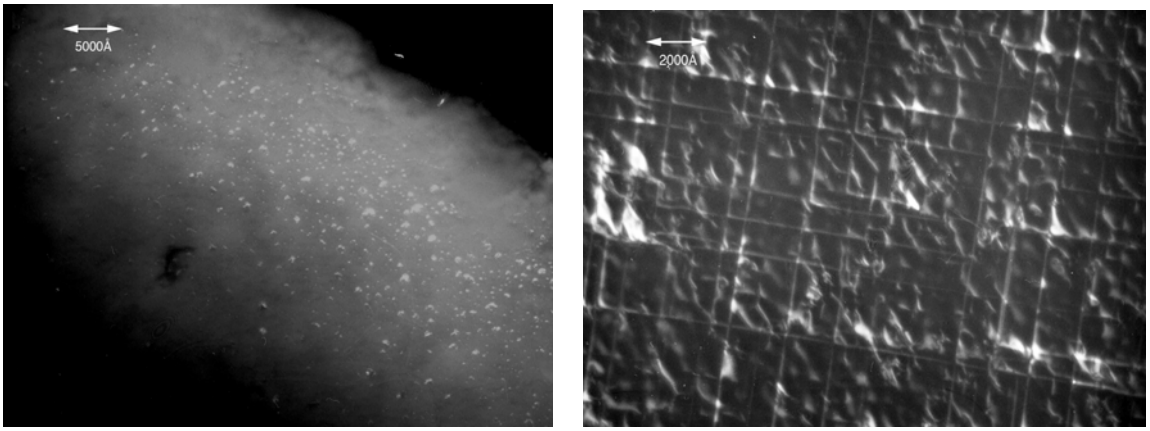


Fig 2.8 Plan view TEM images of epitaxial Ge layers grown directly on Si substrates (left) and using a dislocation blocking layer template (right) clearly illustrate the advantages of using the dislocation blocking layer technique. The Ge grown directly on Si shows significant islanding while the new technique yields a well behaved cross hatch morphology for ultra thin SiGe thicknesses of ~90 nm.

XRD scan of a grown sample (Fig 2.9) shows the presence of multiple peaks corresponding to Bragg reflection from Ge (004) plane in addition to the underlying SiGe layers and the Si substrate. The XRD rocking curves along with the SIMS data show the presence of a pure Ge epitaxial layer.

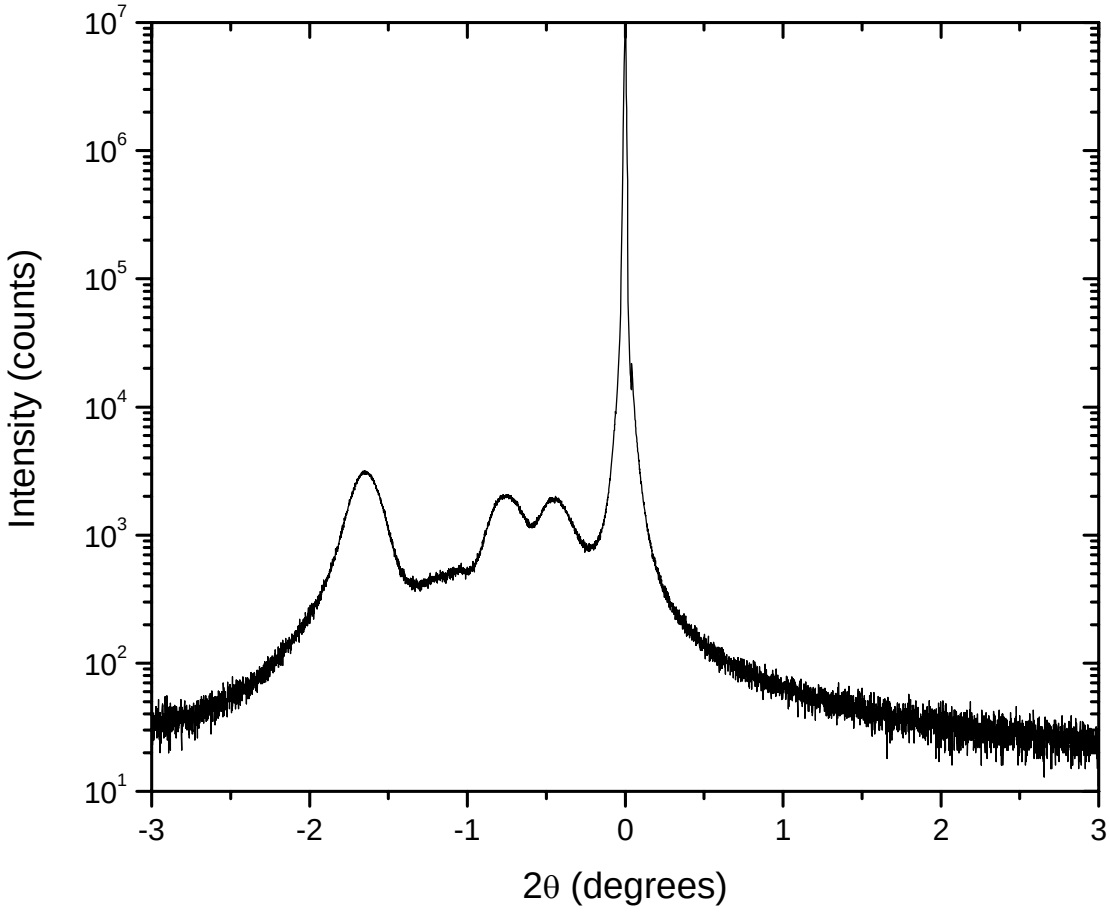


Fig. 2.9 XRD scan of Ge grown using dislocation blocking layers shows multiple SiGe peaks and a strong bulk Ge peak.

Strain analysis using Raman spectroscopy (Fig 2.10), was also done on the grown stack and it was compared with a bulk Ge and a bulk Si sample. The analysis follows Tsang *et al.*[30]. The Ge grown on the thin rapidly-graded SiGe layers showed a Ge-Ge phonon peak which closely matches with the bulk Ge sample showing that the defect free epi Ge layer is slightly compressively strained. In Fig. 2.10, the Raman spectra of the sample without a Si cap layer are shown.

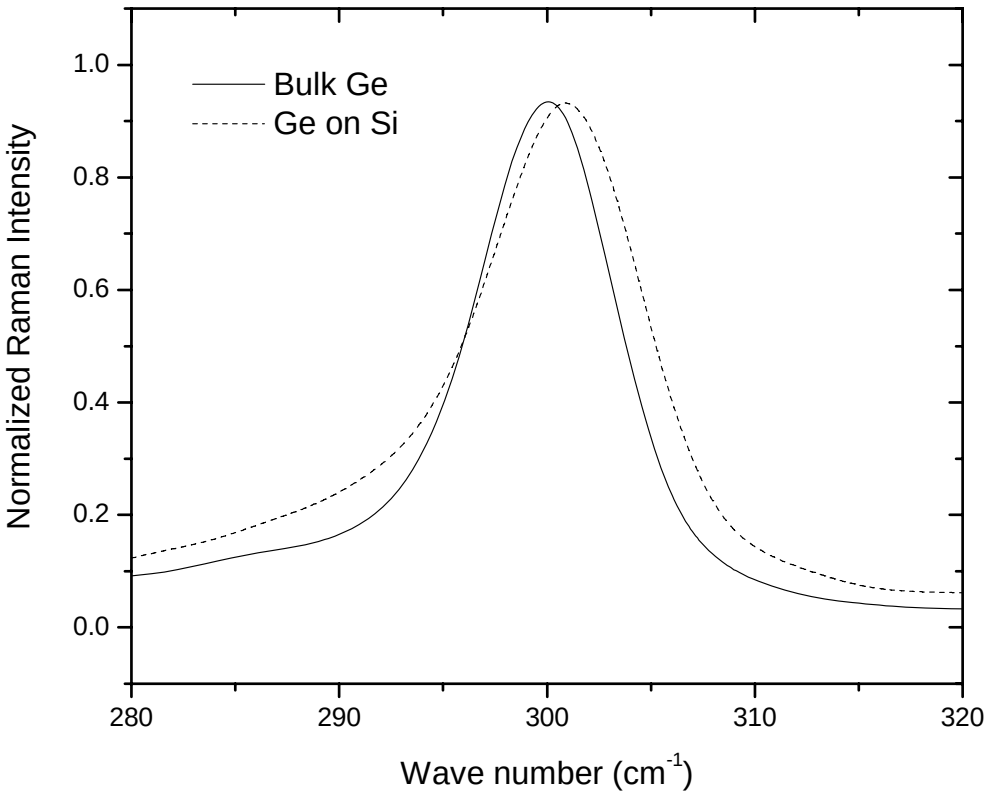


Fig. 2.10 Raman spectra from sample without a Si cap shows well behaved Ge-Ge phonon peak with some possible compressive strain in the Ge.

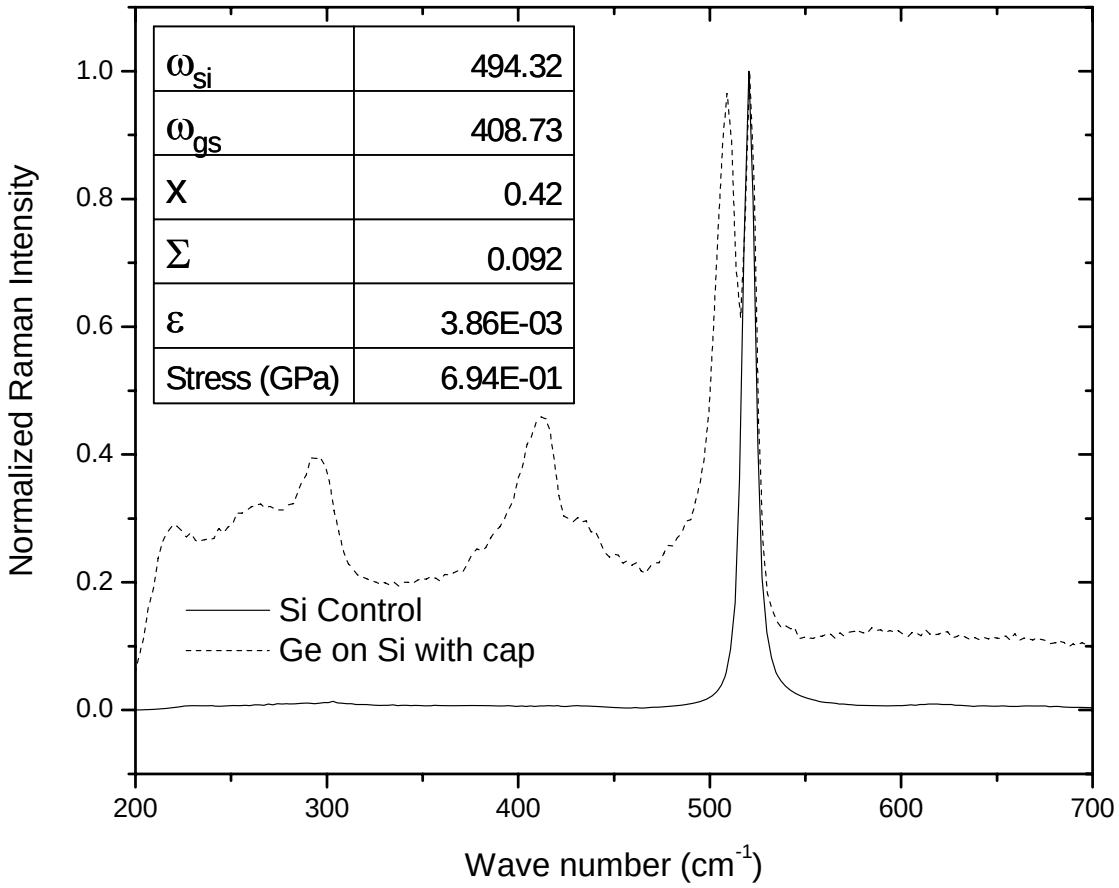


Fig. 2.11 Raman spectra comparison illustrates a double Si-Si phonon peak which may be indicative of a tensile strained Si cap. The Ge-Ge phonon peak shows significant broadening and is attributed to possible strain / partial relaxation of the lower Ge layer after the high temperature Si cap layer growth

For samples with a Si cap layer, some broadening in the Ge-Ge phonon peak was observed which may be attributed to strain relaxation and possible defects after the epi Si cap layer growth at high temperature. In addition this sample also shows a double Si-Si

peak which may indicate tensile strain in the Si cap layer. The Si substrate peak and compressively strained Si-Ge phonon peaks corresponding to the partially strained underlying SiGe layers are also observed. A similar analysis was performed for strained Si layers grown on the dislocation blocking layer template as shown in Fig. 2.12.

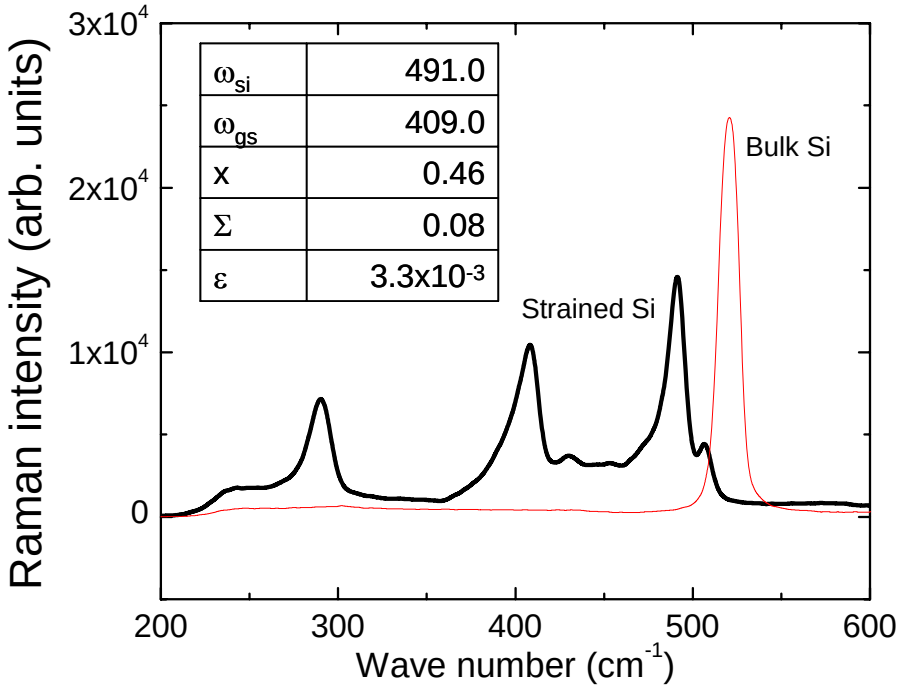


Fig. 2.12 Strain analysis for strained Si grown on dislocation blocking layers shows a strong Si – Si shoulder indicating a tensile strained Si layer, along with phonon peaks for Si-Si, Si-Ge and Ge-Ge bonds in the dislocation blocking layer template.

For the sample shown here, the Ge mole fraction was increased to ~50 % (from SIMS). The Raman spectra show a significant strain and a double peak corresponding to Si-Si phonons in the relaxed SiGe and tensile-strained Si layers, as shown in Fig. 2.12

The lower SiGe layer is almost completely relaxed ($\varepsilon \sim 3.3x10^{-3}$) and the Ge mole fraction is ~ 46% (from Raman spectroscopy) which corresponds to a lattice mismatch of ~ 1.8 %. ω_{Si} and ω_{GS} are the wave numbers corresponding to the Si-Si and Ge-Si phonons in the Raman spectra. X and ε are the Ge mole fraction and relative stress ($\delta l/l$) respectively. This data demonstrates the possibility of incorporating significant levels of strain in the strained Si layer using the dislocation blocking technique. Furthermore, for the strained Si layers, Raman spectroscopy was used to examine the effects of process conditions on the strain and Ge mole fraction in the lower layers.

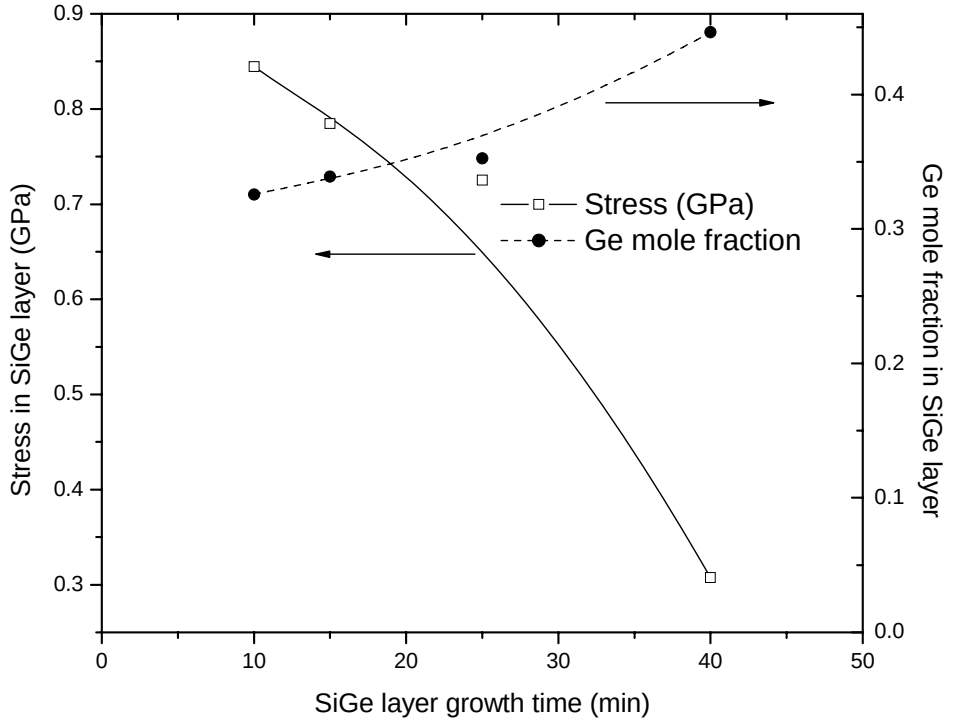


Fig 2.13 Stress and Ge mole fraction in the topmost SiGe layer of the dislocation blocking template as a function of the layer growth time indicate strain relaxation and a gradual increase in the Ge mole fraction.

In Fig 2.13 we show the behavior of stress and Ge mole fraction as a function of the top-most SiGe layer growth time. In general, longer growth times for the $Si_{1-x}Ge_x$ result in further relaxation. The Raman spectra are a superposition of the response from SiGe layers with different mole fractions in close proximity to each other. This may affect the accuracy of the analysis which was performed using models proposed for bulk SiGe layers.

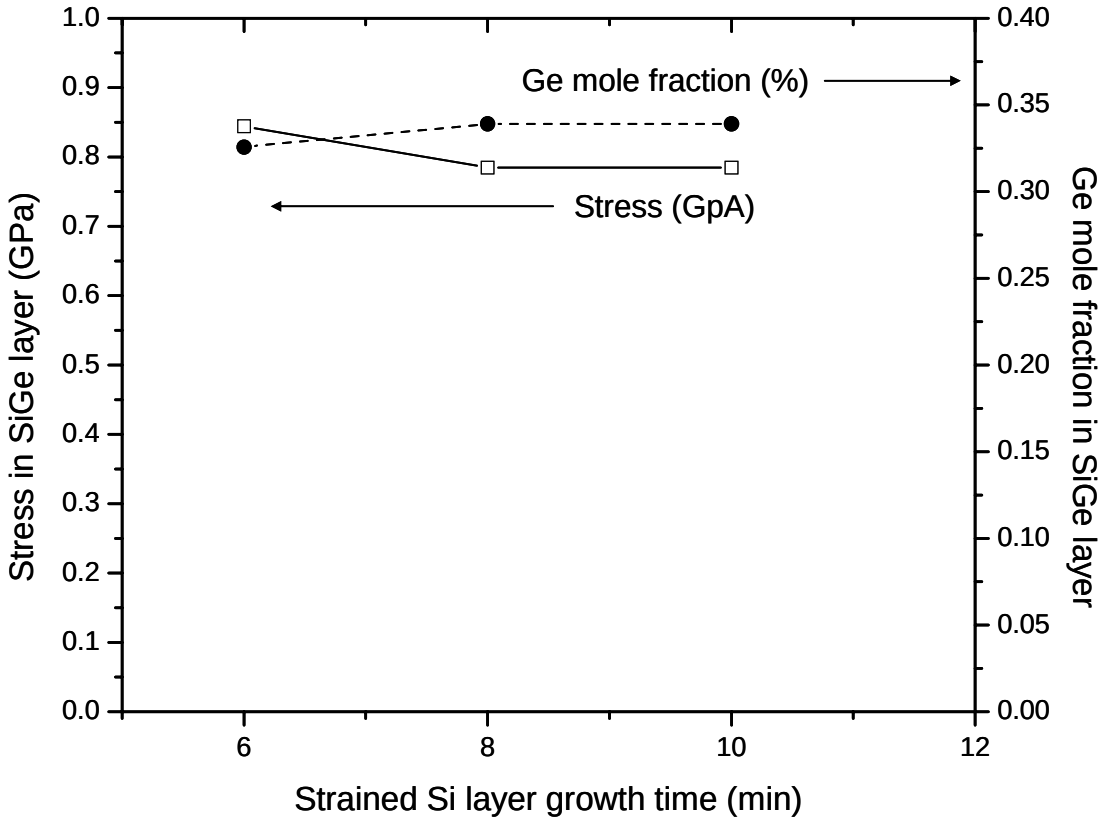


Fig. 2.14 Stress and Ge mole fraction in topmost SiGe layer as a function of strained Si cap layer growth time indicates almost no change in either quantity for the process window considered.

In Fig. 2.14 the strain and Ge mole fraction are compared for different strained Si cap layer growth times. Strained Si layer growth time did not impact the strain and Ge mole fraction or strain levels in the process window considered for our experiments. Overall, Ge mole fraction increases with longer growth times for the lower SiGe layers, possibly due to an incubation time effect, but remains relatively unchanged with the strained Si layer growth time as expected. In order to further characterize the evolution of strain and Ge mole fraction as a function of thermal processing, X-Ray Diffraction (XRD) and Reciprocal Space Maps (RSM) were used to compare the strain and Ge mole fraction in the dislocation blocking layers, before and after a 600 C 30 min anneal in N_2 as shown in Fig 2.15. A comparison of these maps indicates an interdiffusion between the dislocation blocking layers as observed by the merging of the two $Si_{0.8}Ge_{0.2}$ and $Si_{0.75}Ge_{0.25}$. AFM scans did not show any increase in the RMS surface roughness after this anneal.

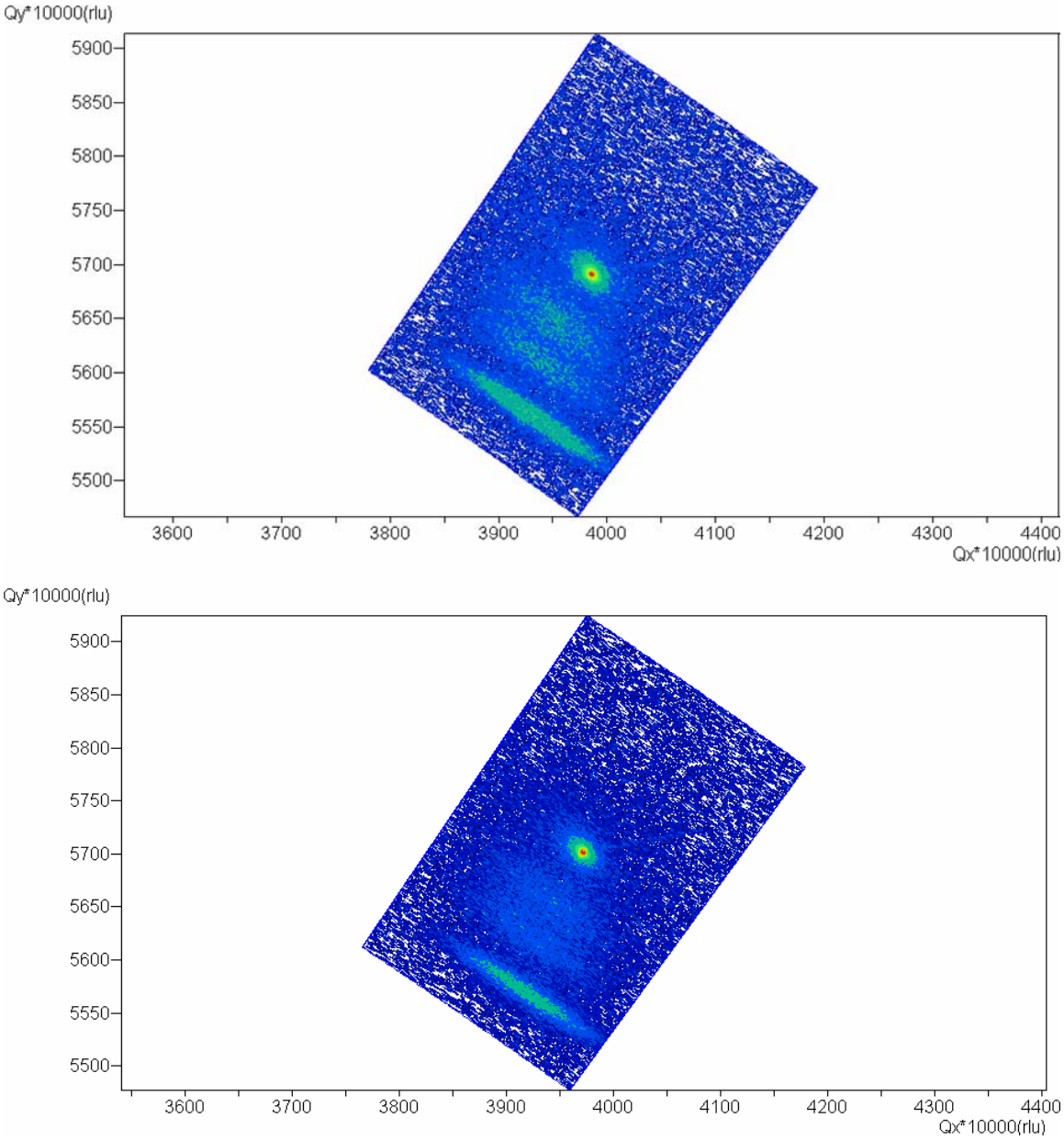


Fig 2.15 Reciprocal space map comparison of dislocation blocking layer before (above) and after (below) a 600^{o} C / 30 minute furnace anneal indicates SiGe interdiffusion and a merging of the two lower mole fraction SiGe peaks.

2.3 DEVICE FABRICATION

Following the epitaxial growth, MOS capacitors were fabricated using HfO_2 (physical thickness ~60Å) and TaN gate stack on a pure Ge sample grown on graded SiGe layer with a Si cap layer in order to characterize the carrier confinement kinks in the CV curves resulting from the valence band offsets (type I) between Si cap and the Ge on thin graded SiGe layers. Both ringFET and conventional geometry MOSFET devices were fabricated on this heterostructure a thin (~5nm) Si cap layer using HfO_2 and TaN as the gate stack. For the first set of PMOS devices, a 25 keV / $5x10^{15}$ cm^{-2} BF_2 implant was used. A deeper 10 keV / $1x10^{15}$ cm^{-2} B implant was used for the next batch to increase the junction depth so that a major portion of the junction lies deeper within the bulk Si substrate. For strained Si NMOS devices, a 50 keV / $5x10^{15}$ cm^{-2} P implant was used to achieve a similar result.

2.4 MOS CAPACITOR CHARACTERIZATION

The Si cap leads to a quantum well resulting from the valence band offset between Si and Ge and the underlying $Si_{1-x}Ge_x$ layers that confines the holes in accumulation. The confined carriers lead to a strong plateau in the CV curve (Fig. 2.16) which is considered a signature of carrier confinement in the Ge layer.

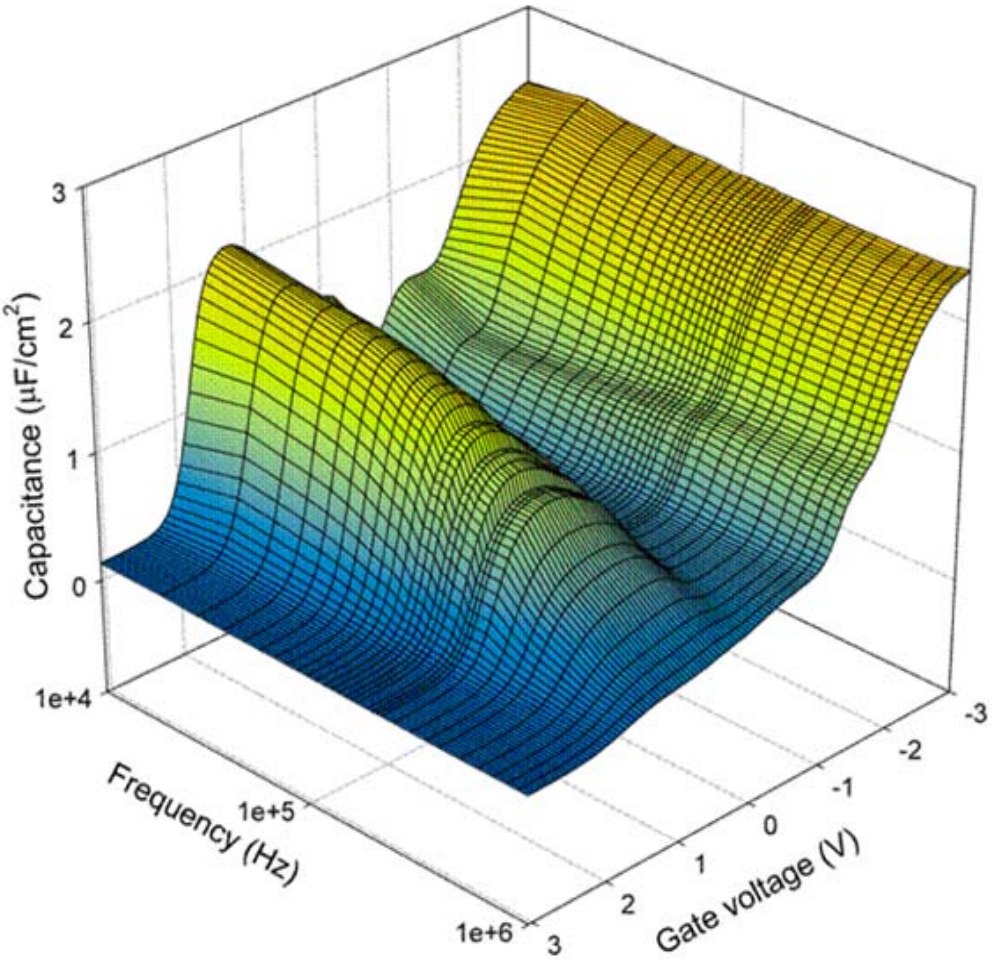


Fig. 2.16 Frequency response of NMOS capacitors indicates a plateau in the depletion region, possibly due to carrier confinement and an enhanced response in the inversion region which was attributed a response from the defects in the dislocation blocking region. The response dies out at high gate biases as the depletion region widens beyond the dislocation blocking layers.

An enhanced response in the inversion region was also observed – this was attributed to carrier generation / recombination at the defects in the dislocation blocking

layers. Once the gate bias extends the depletion region width beyond the dislocation blocking layers, this response is reduced to the regular high frequency response in inversion expected for MOS capacitors. The gate leakage current densities of the MOS capacitors with the Si cap were also satisfactory as shown in Fig. 2.17. Devices without a Si cap layer were severely degraded.

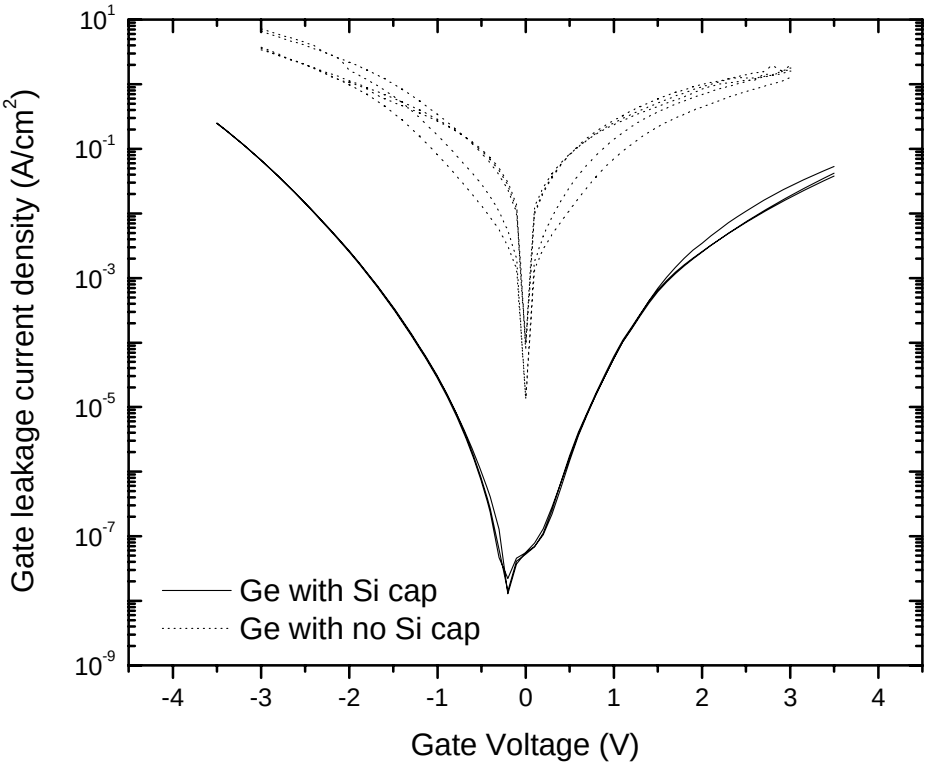


Fig. 2.17 Gate leakage current density comparisons for samples with and without a Si cap layer illustrate a significant degradation of the gate leakage for high k directly on Ge.

2.5 MOSFET CHARACTERIZATION

MOSFETs were fabricated on the tensile-strained Si as well as relaxed Ge layers. For the PMOSFETs, we focus on buried channel devices with a thin (5 nm) Si cap layer. High gate leakage, as shown in Fig. 2.17, dominates devices with no Si cap layer which precludes PMOSFET fabrication on these. Interface preparation for high k materials on Ge has been challenging for the most part and Si passivation has been one of the leading candidates[31]. The two orders of magnitude reduction in leakage observed with the Si cap layer correlates well with the other reported data, but this could be further optimized. We extracted effective oxide thicknesses of ~2nm with gate leakage current of ~$2x10^{-5}$ A/cm^2 at 1V for the pure Ge PMOS samples with the Si cap layer. Initial PMOSFET data was dominated by drain to substrate leakage, possibly due to the diode depletion region probing the defects in the dislocation blocking layer.

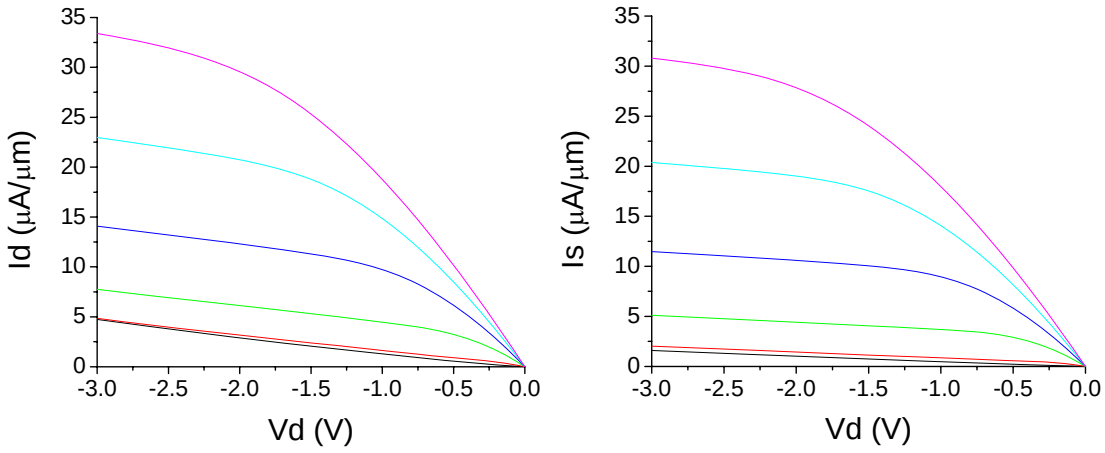


Fig. 2.18 Output characteristics of MOSFETs with a deeper S/D implant suggest that a significant portion of the off state leakage is dominated by drain junction leakage, possibly due to defects in the dislocation blocking layers.

Hence, one of the optimizations to the process included pursuing deeper source drain regions to reduce junction leakage. In the second set of MOSFETs, this helped improve the output and transfer characteristics quite a bit, but no improvement in mobility was observed. The output characteristics for drain and source currents are shown in Fig. 2.18. Transfer characteristics illustrate only about a order of magnitude on / off ratio and are illustrated in Fig. 2.19

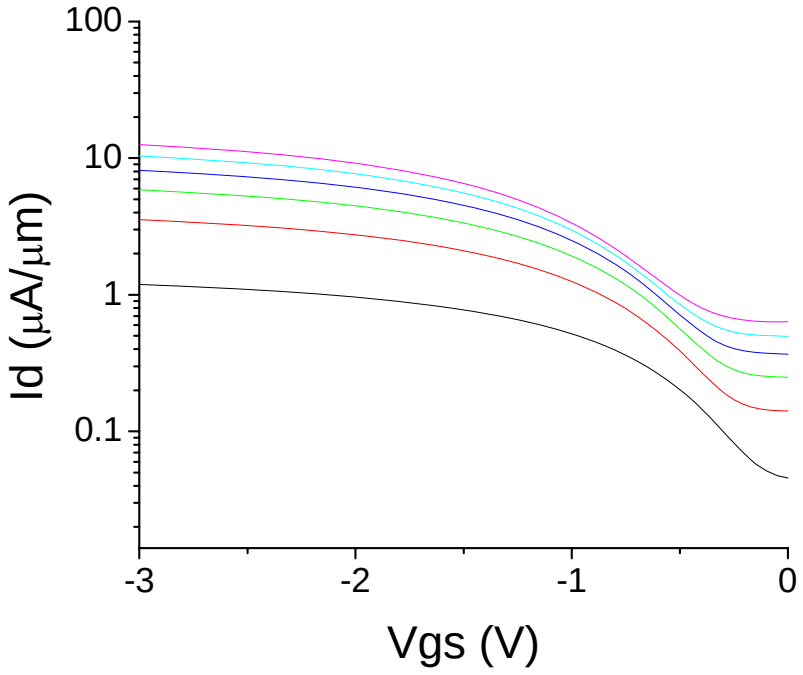


Fig. 2.19 Transfer characteristics of Ge PMOS devices with a 5 nm thick Si cap layer show severe degradation in the subthreshold slope and increase of the off-state leakage at the drain junction.

Later, as will be discussed in chapter 5, the Si cap layer thickness was reduced further to less than 2nm for epitaxial Ge grown on (110) surfaces to achieve hole mobility enhancements of about 3X over universal Si / SiO_2 hole mobility.

NMOSFET results demonstrated ~ 50% improvement in drive current over control Si samples and a mobility enhancement of ~1.8X which is consistent with other experimental[32,33] and theoretical calculations [34,35] reported for strained Si grown on thick relaxed SiGe virtual substrates. Samples with a target Ge mole fraction of 40% and 60% (Ge-4 and Ge-6) in the topmost SiGe layer of the dislocation blocking template were fabricated for this experiment. SIMS results indicate that we achieved about 35% and 50% Ge instead. The output characteristics are shown in Fig. 2.20 A 50% enhancement in the drive current is observed for the Ge-4 sample. The junction was designed to be significantly deeper into the Si substrate using a 50 keV P implant which reduced the off-state leakage as well.

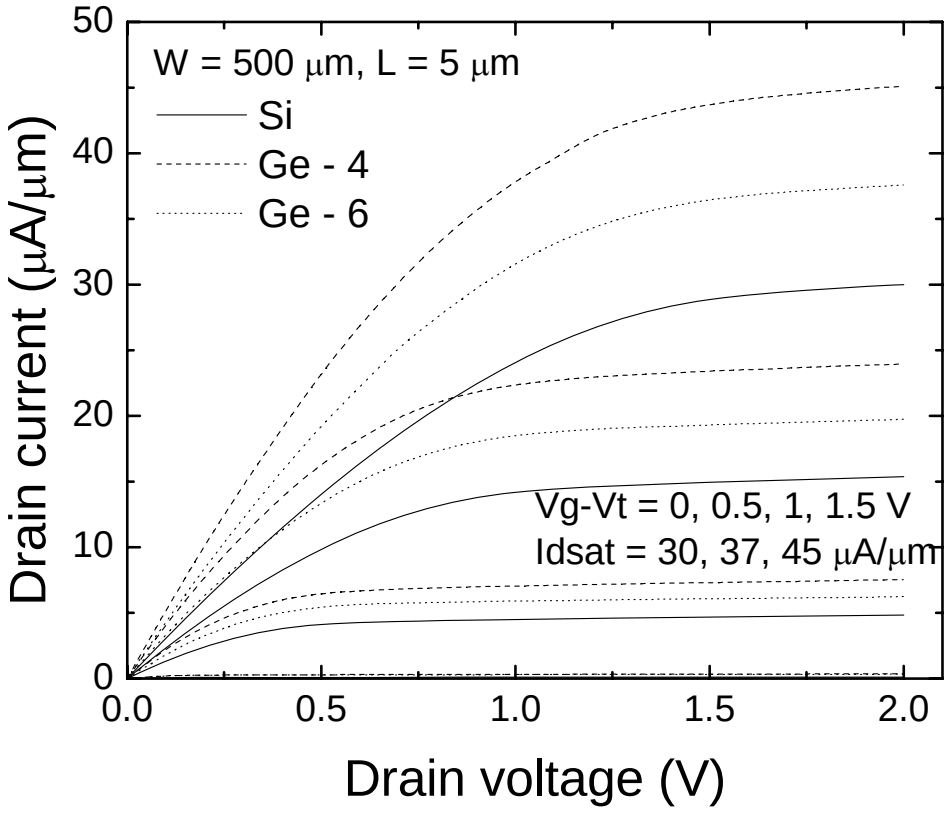


Fig. 2.20 Output characteristics of Ge-4 and Ge-6 sample indicate an enhancement of about 50% for Ge-4 and 33% for Ge-6.

The mobility data is shown in Fig. 2.21 and was extracted from the linear drain current equation.

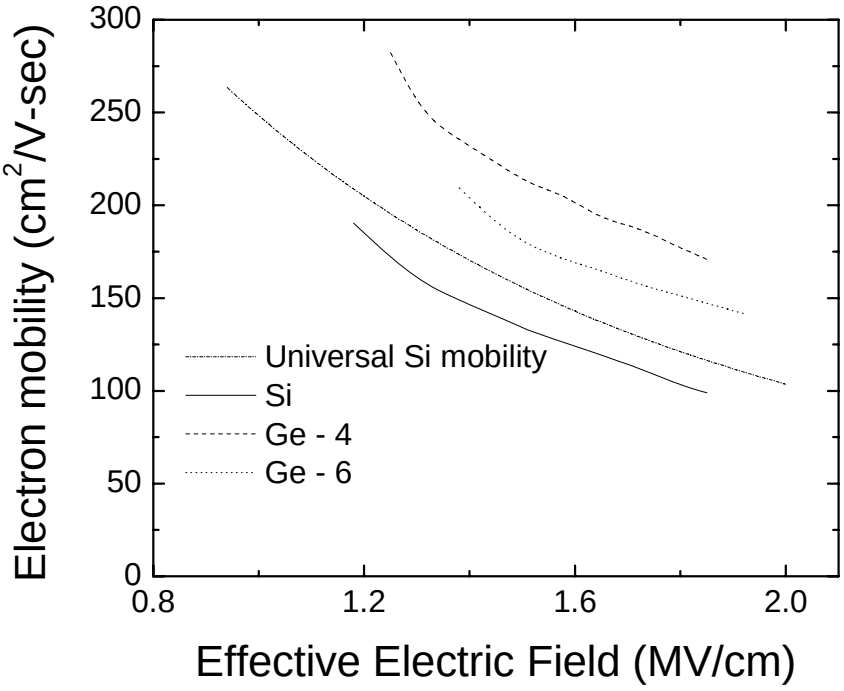
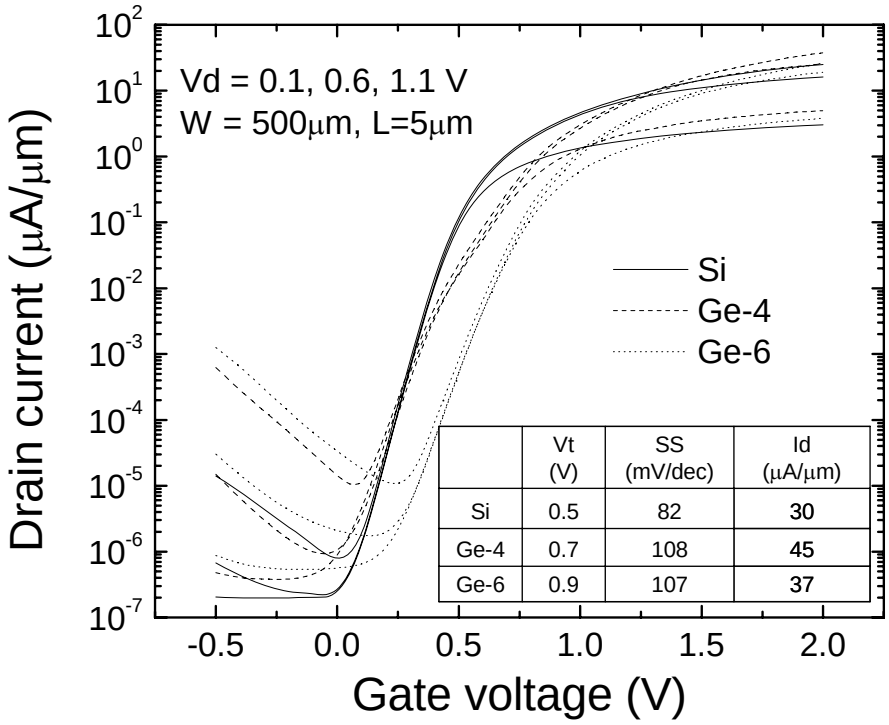


Fig. 2.21 Mobility extraction for strained Si NMOSFETs was performed using the linear drain current equation, and shows a significant enhancement for the Ge-4 sample over universal Si / SiO_2 electron mobility.

Transfer characteristics (Fig 2.22) demonstrate a subthreshold slope of 108 mV / decade and a threshold voltage of 0.7 V. The threshold voltage was significantly high for strained Si, possibly due to fixed charge created during the gate dielectric process and this leads to a fairly high field for mobility extraction.



	Vt (V)	SS (mV/dec)	Id (μA/μm)
Si	0.5	82	30
Ge-4	0.7	108	45
Ge-6	0.9	107	37

Fig. 2.22 Transfer characteristics of strained Si NMOSFETs indicate tradeoffs in subthreshold slope and increased off state leakage which accompanies the drive current enhancement observed for strained Si.

2.6 SUMMARY

This chapter discussed some promising material and electrical characterization results on both Ge channel PMOSFETs and strained Si NMOSFETs using the dislocation blocking layers as a template for channel material fabrication. Significant performance enhancement was observed for lower strain levels used in the strained Si NMOS devices, but a degradation was observed for the Ge devices which may be attributed to excessive lattice mismatch, and resultant strain relaxation and defect formation particularly between

the relaxed Ge and the relatively thick (~5nm) Si cap layer. Devices without any interfacial Si layer result in a significantly higher leakage. Further optimization of the high k / Ge interface for bulk Ge channel devices is discussed in chapter 3 and a similar approach was adopted for devices discussed in chapter 5 for epitaxial Ge on (110) Si substrates. Junction design optimization was discussed for both PMOS and NMOS devices and utilized successfully for the long channel devices discussed in this dissertation, but deeper junctions are obviously not a scaleable way to fabricate short channel MOSFETs. It is envisioned that the top channel layer could be transferred to a silicon-on-insulator configuration which would also help improve device performance since junction capacitance is drastically reduced.

Chapter 3: Interface layer engineering using bulk Ge substrates

3.1 MOTIVATION

As discussed in the previous chapters, along with epitaxial material quality, the other important aspect that impacts the successful demonstration of improved performance on Ge channel devices is the appropriate preparation of the semiconductor / insulator interface. In order to study the semiconductor / insulator system for Ge, the use of bulk Ge substrates is more appropriate since high quality wafers are already available from vendors.

Germanium channel MOS devices have been aggressively pursued for a 4.2X (hole) and 2.8X (electron) bulk mobility enhancement over Si[36,37] for potential introduction beyond the 32 nm technology node. A long channel low field mobility enhancement has also been correlated with improved device performance.[38] The availability of high-κ dielectrics for Si technology, notably HfSiO,[39] provides an opportunity to revisit the poor surface passivation of Ge by its native oxides to achieve high performance, surface channel MOSFETs. Germanium devices fabricated using various high k[40] and interface passivation techniques [41,42,43] perform better than their corresponding Si control devices, but seldom provide significant enhancement over universal Si/SiO_2 hole mobility. High mobility Ge MOSFETs often use a buried channel architecture,[44,45] which exacerbates short channel effects and thus, to a certain extent, negates the aim of introducing Ge channels for nanoscale devices. This chapter focuses

on long channel Ge PMOSFETs using an alternative, deposited SiO_x interfacial layer that yields a mobility of 332 $cm^2\ V^{-1}\ s^{-1}$ at 0.05 MV/cm, a 2X enhancement over universal Si/SiO_2 hole mobility in a surface channel device.

3.2 DEVICE FABRICATION

PMOSFETs were fabricated using a conventional four-mask process flow on Sb-doped (~$5x10^{14}$ cm^{-3}) bulk Ge wafers from Umicore. Plasma enhanced chemical vapor deposition (PECVD) was used to deposit 400 nm of field isolation oxide. Active areas were patterned and etched using optical lithography and a CF_4-based dry etch to remove 350 nm of the PECVD oxide. The remaining PECVD oxide was removed during 1% HF rinse immediately prior to the gate dielectric deposition to minimize the exposure of bulk Ge to the atmosphere. An *ultra-thin* passivation layer of SiO_X was then deposited directly on the Ge surface. SiO_X deposition was immediately followed by HfSiO deposition using an atomic layer deposition (ALD) process described elsewhere[46,47]. WN was used as one of the gate electrode materials in a series of experiments. A 220 nm thick TaN electrode was then deposited on each of these metal gates to form the gate stack. Long channel devices (1 – 100 μm) were fabricated in this experiment. A 10 keV, $1x10^{15}$ cm^{-2} B^+ implant was used to form P^+ source and drain regions. PECVD contact isolation oxide was then deposited. Activation was performed after Al metallization at 400°C for 20 min in an N_2 ambient. This activation anneal is sufficient to provide an $I_{D\text{-}ON}/I_{D\text{-}OFF}$ ratio of 3 x 10^3.

3.3 MATERIAL CHARACTERIZATION

Fig. 3.1 shows scanning transmission electron microscopy electron energy loss spectroscopy (STEM-EELS) and energy dispersive x-ray spectroscopy (EDXS) line scans taken from a MOSFET.

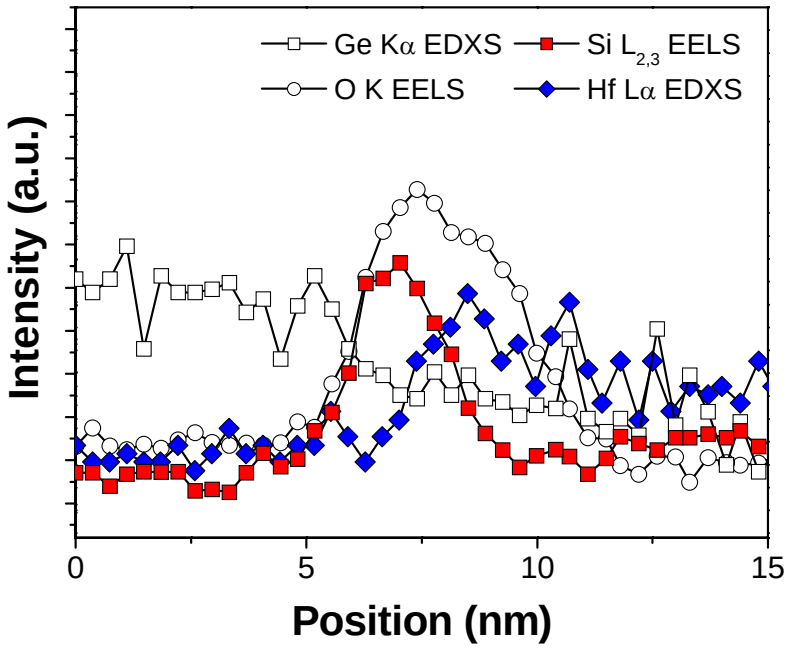


Fig. 3.1 STEM-EELS and EDXS scans on a bulk Ge / SiOx / HfSiO / WN gate stack indicate an overlap between the Si and O profiles, suggesting complete oxidation of the deposited silicon. Presence of Ge in the HfSiO cannot be ruled out.

The Si and O profiles overlap at the interface with Ge suggesting that a SiOX passivation layer directly on Ge was achieved. Based on the EDXS data, the presence of Ge in SiOx and HfSiO cannot be ruled out. The amorphous SiO_X interlayer and the

amorphous HfSiO are believed to slow Ge diffusion into the high k[48]. Segregation of Ge from SiO_2 is also well documented[49]. The high resolution cross sectional transmission electron micrograph (HRXTEM) image shown in Fig. 3.2 further indicates an abrupt Ge/SiO_X interface and 1.6 nm of SiO_X in the gate stack.

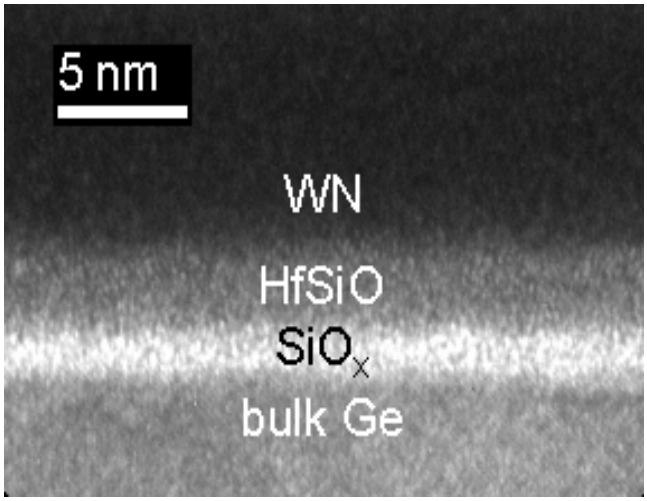


Fig 3.2 High resolution cross sectional TEM image of the gate stack from a fully processed MOSFET indicates a well defined SiO_X interface between the bulk Ge channel and the HfSiO.

X-ray photoelectron spectroscopy (XPS) data on companion monitor wafers also confirmed the absence of elemental Si in the sample. Ge in both elemental and oxidized forms was observed. Indeed, Ge-O bonds are expected at the interface between Ge and SiO_X if the Si is completely oxidized. The combined physical characterization data indicate a surface channel Ge device. While the buried channel architecture may improve mobility vs. a surface channel FET, it is not scalable due to exacerbated short channel

effects and may have limited relevance beyond the 32 nm node. The narrow band gap of Ge may allow supply voltage to be scaled further and reduce short channel effects.

3.4 MOS CAPACITOR CHARACTERIZATION:

Fig. 3.3 shows the capacitance voltage (C-V) characteristics measured on a MOSFET. Hysteresis of 100 mV was observed, which is significantly less than that reported for HfO_2 on GeON interfaces[50,51]

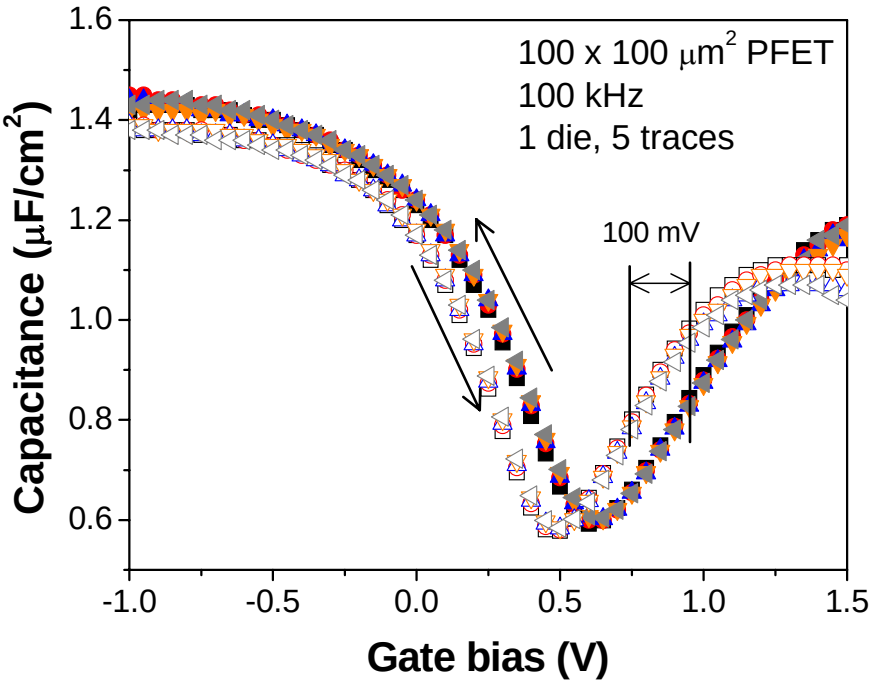


Fig. 3.3 High frequency CV data from a MOSFET with source / drain terminals grounded indicates a hystersis of 100 mV. The accumulation capacitance is observed to roll off at higher gate biases, and this is attributed to gate leakage dominating the measurement in accumulation. Gate leakage in inversion (negative gate bias) is lower. The C_P-D model was used.

Frequency dispersion as shown in Fig 3.4 is negligible between 1 and 100 kHz.

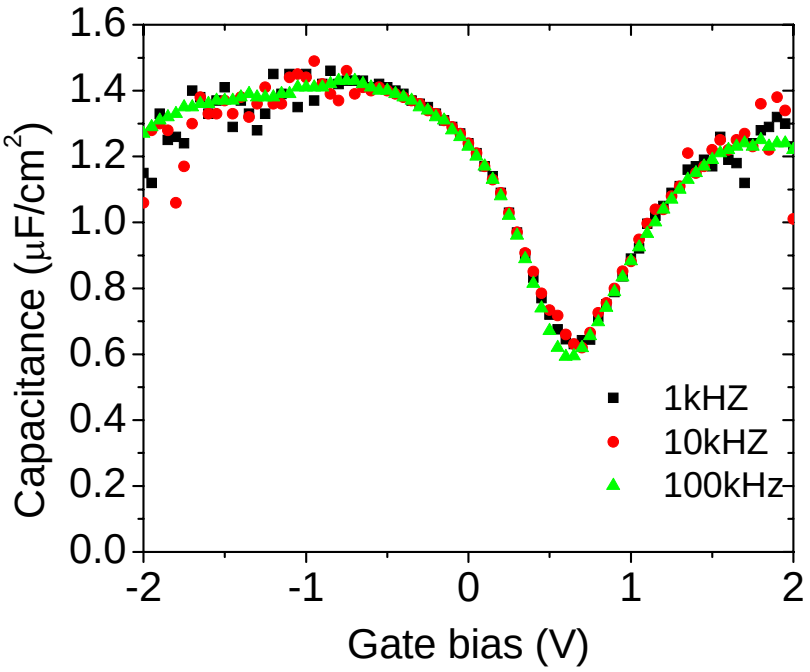


Fig 3.4: Negligible frequency dispersion is observed between a 100 kHz – 1kHz measurement range. For higher frequencies, a significant series resistance and consequently much lower capacitance was seen. For frequencies lower than 1 kHz, the measurement is dominated by gate leakage.

Such promising results are attributed to the adequate passivation of Ge surface states by a wide band gap SiO_2-like overlayer, which may act as a barrier between the substrate and eventual trapping centers. Excellent hysteresis results for samples with HfSiO on Si(100) lead us to speculate that the origin of the hysteresis may not be due to bulk trapping in the HfSiO, but rather due to "border traps"[52] at the SiO_X/HfSiO interface. The Berkeley QMCV simulation code[53] was modified for Ge and used to

estimate a gate stack equivalent oxide thickness (EOT) of ~1.85 nm from the fit to the MOSCAP C-V characteristics[54] as shown in Fig. 3.5. Table 3.1 indicates the parameters used for Ge.

Electron			
Ellipsoid	[111]	[100]	
Surface	{100}	{100}	
Degeneracy	4	2	4
Normal mass	0.120	0.950	0.200
Conductivity mass	0.152	0.200	0.330
Density of state mass	0.299	0.200	0.436
Split energy	0.000	0.190	0.190
Hole			
Band	Heavy hole	Light hole	Split-off band
Degeneracy	1	1	1
Band curvature mass	0.3	0.062	0.079
Density of state mass	0.43	0.014	0.025
Spin-orbit split energy	0.29		

Table 3.1 Parameters used for modifying the Berkeley QMCV code for Ge.

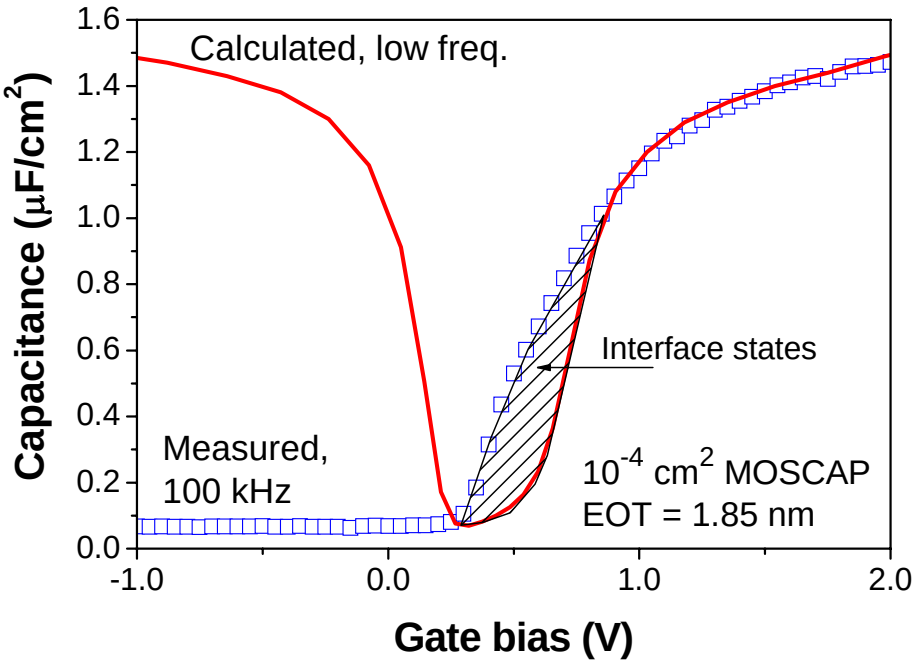


Fig. 3.5 Well-behaved high frequency CV data was observed from MOS capacitors. An effective oxide thickness of 1.85 nm was extracted using the modified simulation program.

An interface state density (D_{IT}) of ~1x10^{13} cm^{-2}eV^{-1} close to mid-gap was extracted using the statistical model of the conductance method, as shown in Fig. 3.6 which is considered to be one of the most sensitive methods to determine D_{IT}.

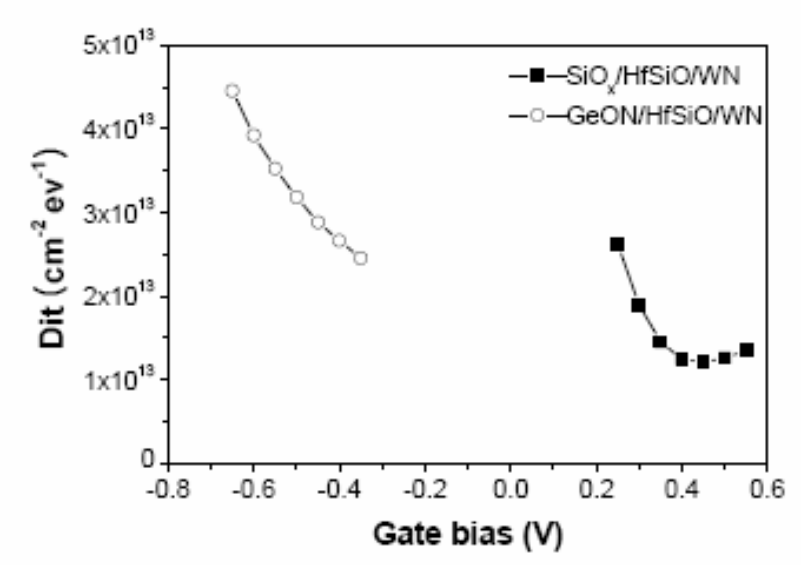


Fig. 3.6 Interface state density extraction for Ge / high k gate stacks with two different interfaces– SiO_X and GeON illustrate a significant reduction achieved by the use of a SiO_X interface as compared to nitridation. A significant shift in the flat band voltage was observed which may be attributed to different process-dependent fixed charges.

While the interface state density is significantly high, it is lower than that reported from similar measurements on a high performing $Ge/Si/SiO_2/HfO_2$ stack.

3.5 MOSFET CHARACTERIZATION

Fig. 3.7 shows well behaved output characteristics, with flat drain current in the saturation region.

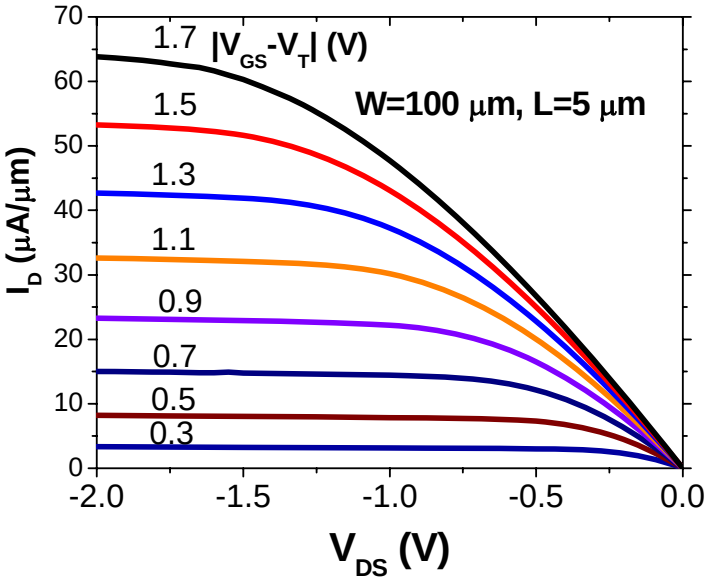


Fig. 3.7 Well behaved output characteristics were observed on a 5um PMOS device.

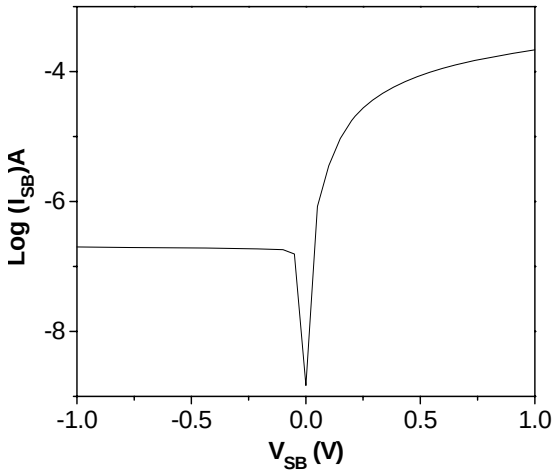


Fig. 3.8 Junction leakage between drain and substrate results in an I_{ON}/I_{OFF} ratio greater than 3 orders of magnitude which is necessary for well behaved output and transfer characteristics.

Junction leakage is shown in Fig. 3.8 and indicates that most of the off state leakage is due to drain-to-substrate leakage as expected for long channel devices. Fig. 3.9 shows transfer characteristics indicating an I_{ON}/I_{OFF} ratio of about $3x10^3$ and a subthreshold slope of 168 mV/dec. Even though high quality junctions allow for a discussion of the actual *drain* current as opposed to the often shown source current, subthreshold conduction is still dominated by junction leakage. Subthreshold slope extracted using the *source* current instead of the drain current is significantly lower: 96 mV/dec.

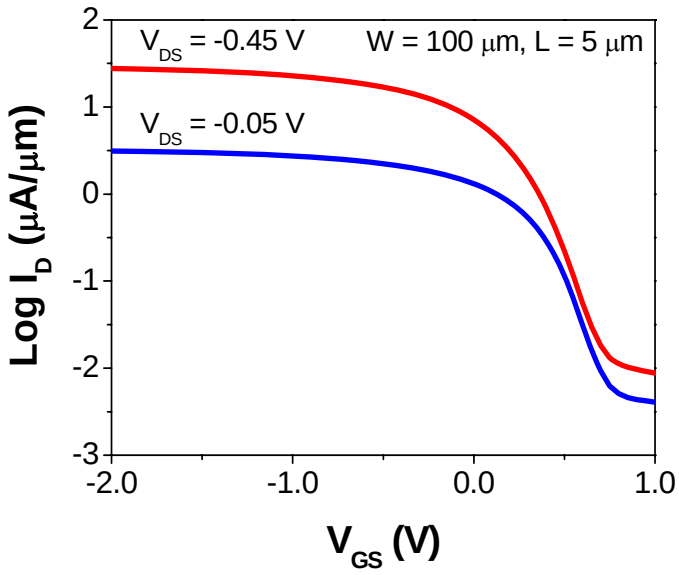


Fig. 3.9 Drain current transfer characteristics of Ge PMOS devices illustrate reasonable on / off behavior and a subthreshold slope of 166 mV / decade.

A steep subthreshold slope and low C_{IT} are consistent with the significantly high mobility observed from DC I_D-V_G and split C-V measurements. However, AC conductance measurements still indicate a significant D_{IT}. These may be attributed to

"border traps"[54] within the SiO_X and/or at the SiO_X/HfSiO interface. These defects, though observed in a gate conductance measurement, would not interfere strongly with DC device performance, thus allowing the high hole mobility observed in these devices. Single pulse I_D-V_G measurements showed no drain current degradation as shown in Fig. 3.10, indicating minimal fast transient charge trapping; this could mean that the C-V hysteresis is primarily due to trapping at or close to the SiO_X/HfSiO interfaces rather than in the bulk of HfSiO. This is currently under further investigation.

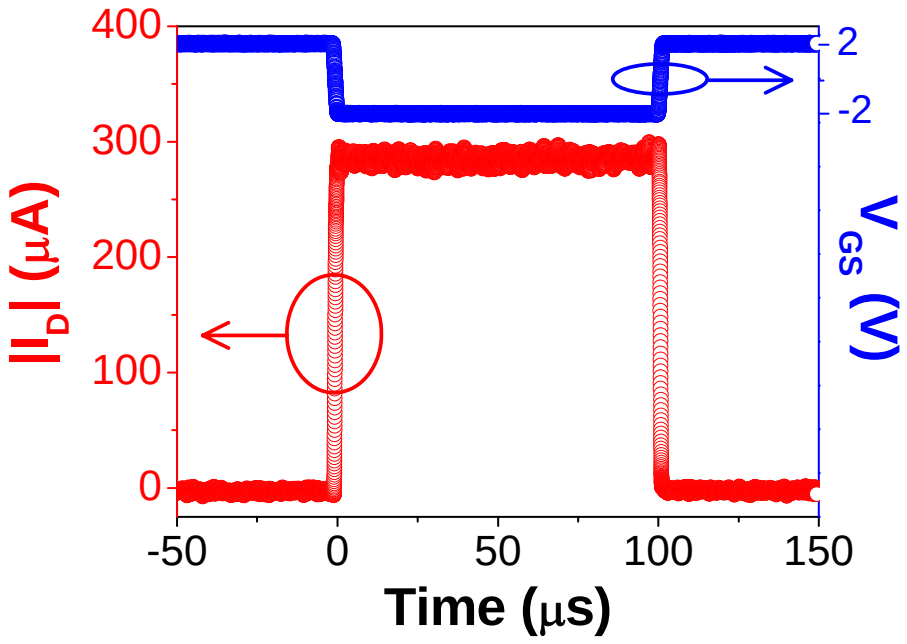


Fig. 3.10 Pulsed I_D-V_G measurements indicate a minimal transient charge trapping which is consistent with the observed high mobility. Hysteresis in the CV data is however inconsistent with the transient charge trapping data and is attributed to border traps at the SiO_X / HfSiO interface.

Effective mobility was extracted using the split C-V technique. A peak mobility of 332 cm^2 V^{-1} s^{-1} at 0.05 MV/cm was observed as shown in Fig. 3.11.

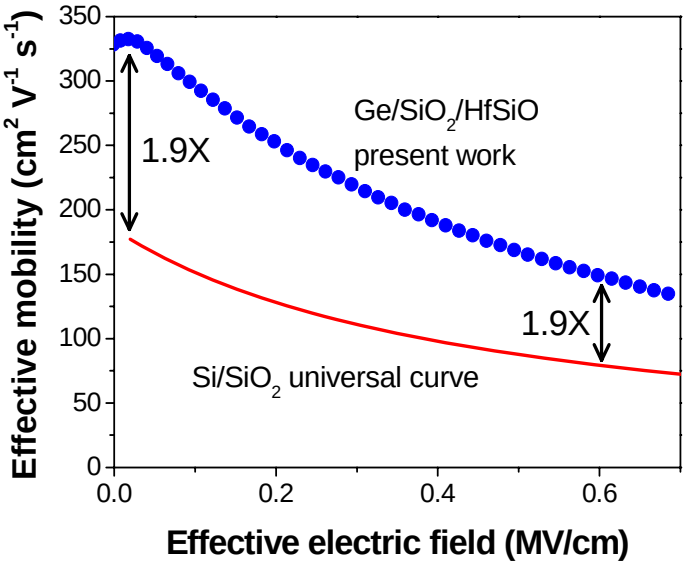


Fig. 3.11 Mobility extraction performed using split CV measurements shows a peak mobility of 332 cm^2 / V-s. Depletion charge was calculated using the substrate doping. A correction for overlap capacitance was applied for the inversion charge measurement.

This is an enhancement of 1.9X over the universal Si/SiO_2 mobility. Significant enhancement (~1.9X) is retained at fields as high as 0.7 MV/cm. The equations used for mobility extraction are shown below.

$$Q_{depl} = \int C_{depl} \times dV_{GS}$$

$$Q_{inv} = \int C_{inv} \times dV_{GS}$$

$$E_{eff} = (\frac{1}{\varepsilon_{ge}})(Q_{depl} + \frac{Q_{inv}}{\eta = 2})$$

$$\mu_{eff} = \frac{L}{W} \times \frac{I_D}{Q_{inv} \times V_{DS}}$$

This significant mobility enhancement can be achieved with adequate interface quality coupled with a high-k material that is capable of 90% universal SiO_2 mobility on Si(100).[4] To our knowledge, this is one of the highest mobility values reported on unstrained surface channel Ge devices as detailed in table 3.2.[55,56,57,58,59, 60, 61]

Gate stack on Ge	Max. μ_h ($cm^2 V^{-1}s^{-1}$)	EOT	Device	μ_h extraction	D_{IT} ($cm^{-2}eV^{-1}$)	S.S. (mV/dec)	Ref.
SiO_X/HfSiO/WN	332	1.8	MOSFET	split CV	$1x10^{13}$	96 (I_S)/168	This
ZrO_2/Pt	313	0.6-	ringFET	$I_{D,LIN}$ eqn.	N.A.	N.A. (I_D)	55
Si/SiO_x/HfO_2/TaN	250	1.4	MOSFET	split CV	$2x10^{11}N_I$	N.A. (I_S)	56
GeON/LTO/Al	310	8.0	ringFET		$5x10^{11}$	82 (I_S)	57
ZrSiO/Mo	230	2.0	—	—	N.A.	99 (I_S)	58
GeON/HfO_2/TaN	200	1.8	MOSFET	split CV	N.A.	80 (I_S)	59
SiO_x/HfO_2/TaN	194	1.5	ringFET		N.A.	N.A. (I_S)	60
Si/SiO_2/HfO_2/TaN	170	2.6	MOSFET	split CV	$5x10^{11}N_I$	N.A. (I_S)	61

Table 3.2 Comparison of reported mobility data on unstrained Ge channel PMOS devices

It is also important to consider the subtle differences between two idealized alternative device configurations:

1. SiO_2 *directly* on a Ge surface

2. One or two monolayers of epitaxial Si on Ge and a SiO_2 layer on top

Both of these approaches are, in principle, very similar to each other and have been successfully implemented for enhanced hole mobility demonstrations. The current results indicate that the SiO_X approach may in fact be more beneficial for high performance Ge MOSFETS. However, further investigation is required before the presence of a few monolayers of unoxidized Si at the top of the channel can be suggested as a possible reason for some mobility degradation. The current results definitely corroborate the well known Si/high k result: the presence of a high band gap SiO_2-like interfacial layer improves mobility.

3.6 RELIABILITY CHARACTERIZATION

Gate leakage shown Fig. 3.12 is comparable to benchmark data for Ge[62]. Gate leakage current density on these devices was fairly low, consistent with the 1.8 – 2 nm EOT observed for these samples.

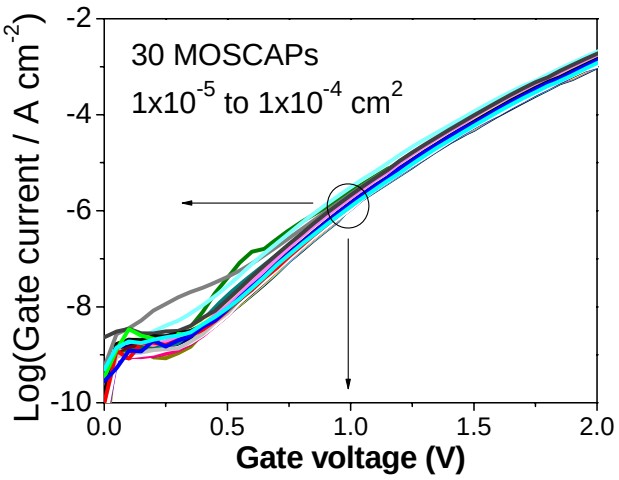


Fig. 3.12 Gate leakage current density was fairly low and tightly distributed across the wafer, consistent with the thicker EOT and an optimized ALD process.

Tightly distributed dielectric breakdown was observed from time zero dielectric breakdown measurements as shown in Fig 3.13 with a breakdown voltage of about 4V in accumulation.

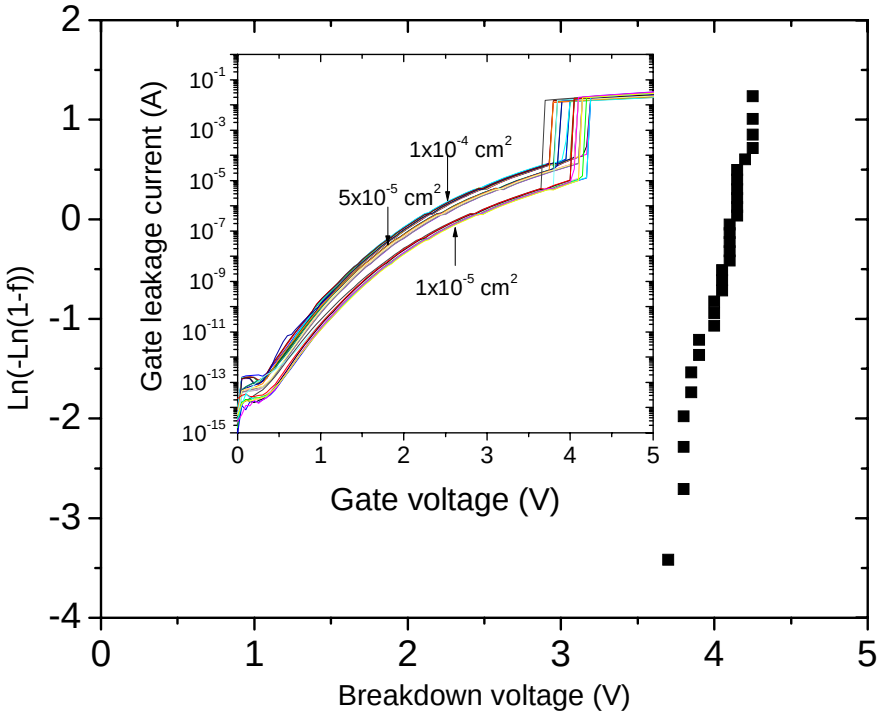


Fig. 3.13 Time-zero breakdown measurements show a tightly distributed Weibull plot with a breakdown voltage of about 4V. The raw IV data is shown in the inset.

Initial negative bias temperature instability data indicate a degradation of 20 mV after a 5000 sec stress at 1.8V as shown in Fig. 3.14. This is one of the first demonstrations of NBTI measurements on Ge devices but further optimization may be possible.

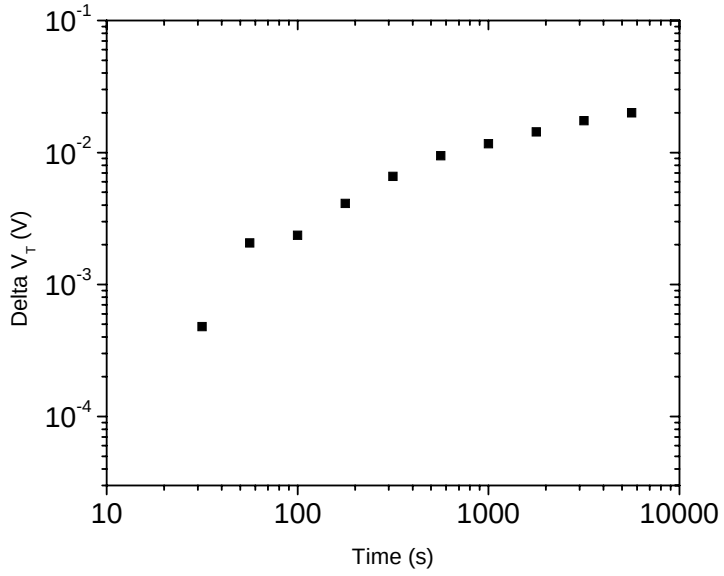


Fig. 3.14 NBTI measurements indicate a V_T degradation of 20 mV after 5000 sec of stress at 1.8V.

3.6 SUMMARY

This chapter discussed experiments targeted towards the optimization of the Ge / high k interface. An alternative approach involving the deposition of an ultra-thin SiO_X layer between the Ge and high k materials without the use of epitaxial growth was demonstrated and a mobility enhancement of over 1.9X was achieved as compared to universal Si / SiO_2 hole mobility. The use of epitaxy to form an optimized Si cap layer, which was, in turn, oxidized to form a similar SiO_X layer for epitaxially grown Ge on (110) Si substrates is discussed in chapter 5, and the work in this chapter was successfully leveraged for subsequent experiments.

Chapter 4: Hybrid crystal orientation Si Mosfets for PMOS performance enhancement

4.1 MOTIVATION:

Hybrid Orientation Technology (HOT)[63] has recently generated a lot of interest in the MOSFET device and technology community due to the significant performance boost provided by the use of different surface orientations for N and P channel MOSFETs. (100) and (110) surfaces were shown to be optimal for N and P channel MOSFETs, respectively, and a current flow in the <110> direction provides the highest drive currents for both types of devices [64,65,66]. As part of this work, a 40% enhancement was observed in short channel PMOS devices on DSB and bulk Si (110) wafers, as shown in Fig. 4.1.

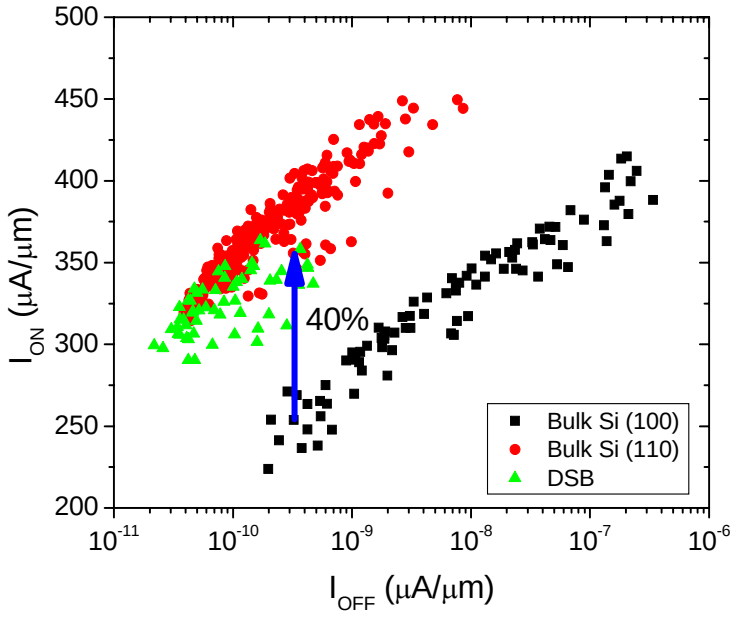


Fig. 4.1 I_{ON}/I_{OFF} performance for PMOS devices shows a 40% improvement in both DSB and bulk (110) samples.

Various implementations of this technology have been demonstrated using Silicon-on-Insulator (SOI) substrates with either one[67] or both[68] types of devices on an insulating layer. But, these solutions proposed for the implementation of HOT on SOI, require selective epitaxial growth which involves significant process complexity and cost. Also, in order to easily reuse circuit design libraries from the bulk CMOS environment, a "bulk-like" technology is of significant interest. One practical way to obtain such hybrid devices in close proximity to each other on bulk-Si-like substrates involves the direct bonding of Si layers of two[69,70] or more[71] orientations to each other. The implementation of such a high performance bulk Si technology mitigates significant technological issues involved in a migration to SOI-based HOT devices and provides a viable bulk alternative. Ultra-thin DSB layers are ideal in order to implement the straightforward scheme of amorphization followed by templated recrystallization (ATR) before shallow trench isolation (STI) proposed by Saenger *et al*.[7] Thinner DSB layers help minimize the triangular morphology observed at the border of the recrystallized region. The final (100) / (110) interface at the border of the re-grown region is defined by the growth characteristics of the specific crystal orientation contributing to the competing SPE. This morphology was observed to be as large as 110 nm for a 100 nm DSB layer and is considered to be a major limiting factor for implementing the DSB-HOT technology at the 45 nm node and beyond for SRAM cells. For this application, the STI areas in current technologies are already smaller than 150 nm and hence there exists a significant thrust for the implementation of ultra-thin DSB layers.

Implementation of ultra-thin DSB layers however creates considerable PMOS device issues. Off-state PMOS leakage is adversely impacted if the bond interface lies close to the junction depletion region. Significantly high off-state leakage for short channel (85 nm) devices fabricated on DSB layers thinner than 100 nm was observed. Thus, upper and lower limits for DSB layer thickness, as dictated by STI scaling and PMOS leakage, are obviously in conflict.

This situation requires the concomitant implementation of process techniques to minimize the triangular morphology and alternative junction engineering to curtail junction leakage associated with defects at the bond interface. Experiments to study the performance of the DSB system as function of DSB layer thickness were performed. Concomitantly, an alternative approach of passivating the (110) / (100) interface by the use of H2, F and N implants was also studied to minimize junction leakage in ultra thin DSB layers.

4.2 CHARACTERIZATION OF THE (110) / (100) BOND INTERFACE

Significant advances in wafer bonding technology have been achieved after the firs commercialization of SOI technology using wafer bonding. For the DSB experiments, all wafers were provided by MEMC Electronic Materials. In the initial stages of the project, the focus was on the optimization of the bond interface to reduce the interfacial oxygen at the (110) / (100) bond interface[72]. The techniques utilized for this process are proprietary. The bonding process is still considered hydrophilic even when oxygen concentration at the bond interface is comparable to the background concentration in the substrate. Such interfacial contamination which would inevitably

impact device performance in areas such as thermal and electrical conductivity across the bond interface and junction leakage if the source / drain depletion regions of the device are close to the bond interface. The interface was characterized by both electrical and material characterization techniques. As shown in Fig. 4.2, X Ray Reflectivity was used to observe fringes in the scan which are attributed to the presence of an interfacial layer when a sample with a SiO_X interface was probed. For the case of an optimized sample, no reflectivity fringes were observed which indicates the absence of any significant SiO_X layer at the interface.

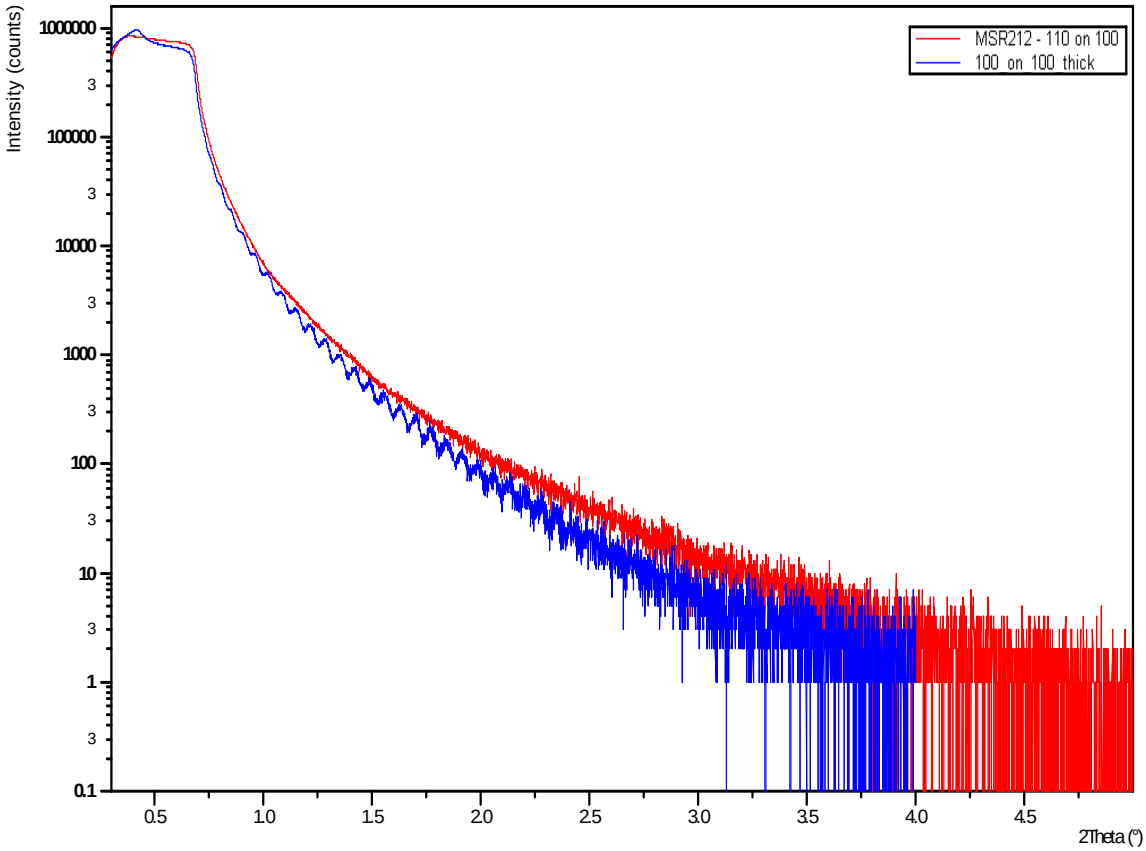


Fig. 4.2 X-Ray Reflectivity characterization of DSB samples with (Blue) and without (Red) an interfacial oxide layer clearly indicates the absence of reflectivity fringes for the optimized sample.

Apart from this preliminary examination, both SIMS and HRXTEM were used to examine the interface. In Fig. 4.3, the SIMS profiles for O and C are shown below for samples with and without an intentional SiO_X interfacial layer. For the optimized bonding process oxygen levels comparable to the background contamination in the substrate of about $5x10^{18}$ cm^{-3} were obtained, which is also the detection limit of the SIMS set up used.

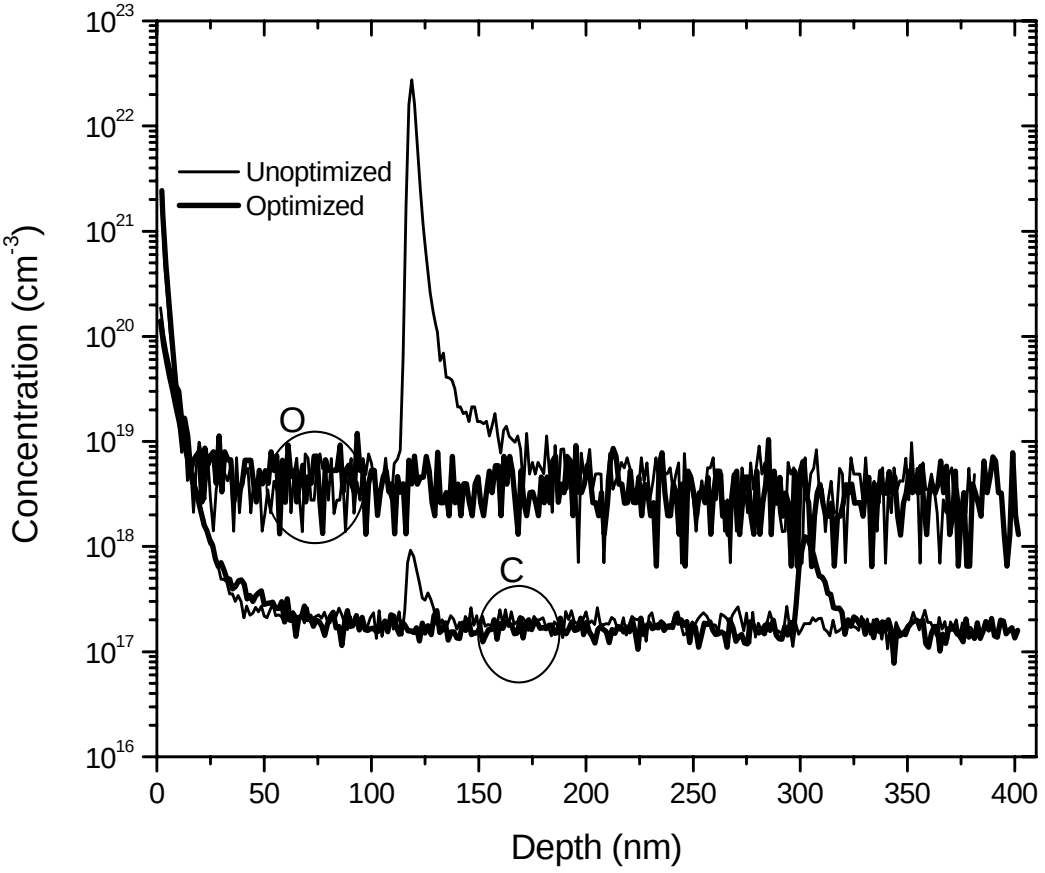


Fig. 4.3 SIMS profiles for C and O for DSB samples with and without an interfacial oxide layer indicate the complete removal of interfacial oxygen for an optimized bonding process. The spike in the C profile serves as a marker for the interface.

HRXTEM imaging indicates significant differences when the bonded crystals are observed in directions parallel and perpendicular to the wafer notch. This was attributed to the near ideal matching of the atomic spacing in the <110> direction of the DSB layer but not in the <100> direction (Fig 4.4).

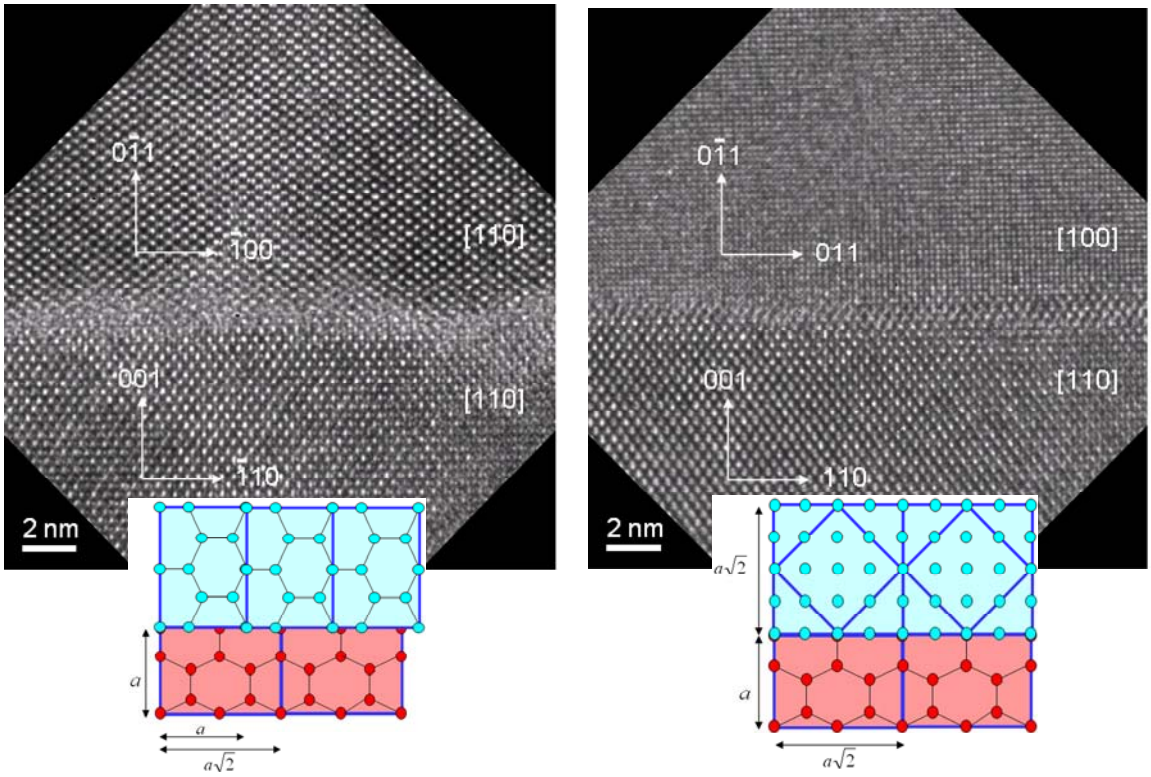


Fig. 4.4 HRTEM images perpendicular (left) and parallel (right) to the wafer notch (both are <110> directions for the bulk Si (100) handler wafer) show clear differences in the bond interface which may be attributed to the possible lattice mismatch, as illustrated in the schematics.

Along with the material characterization, electrical measurements were also performed on vertically-oriented, resistor-like devices using Al and Au electrodes

fabricated on bulk (100), bulk (110) and various configurations of DSB substrates to understand and optimize interface preparation. A schematic of the device is shown in Fig. 4.5.

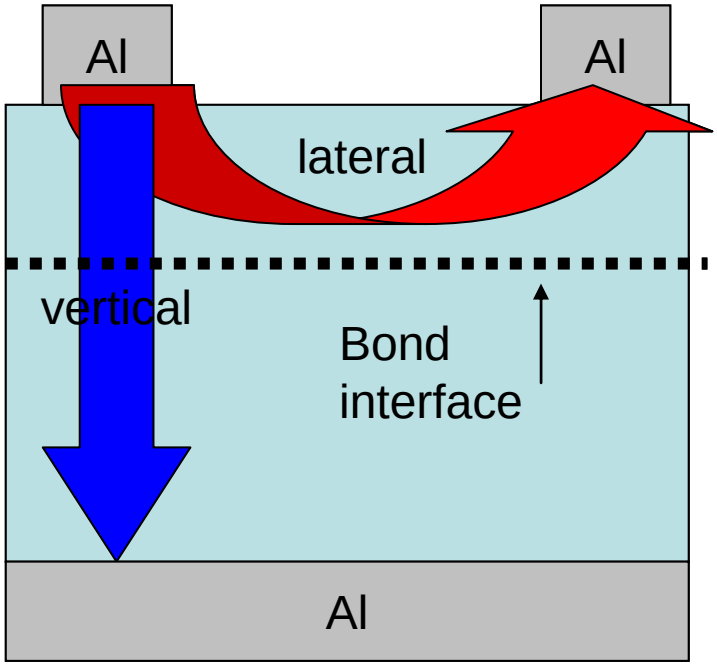


Fig. 4.5 Schematic device structure used for electrical characterization of the (110) / (100) bond interface. Both lateral and vertical IV measurements were performed. Vertical measurements show non-linear IV behavior, while lateral measurements show an increase in the resistance.

For vertical resistor fabrication, the substrates were first cleaned in a H_2O_2 / H_2SO_4 (piranha) / HF last solution. Aluminum was then sputtered, patterned and etched using optical lithography and a wet etch on the front side. The back side of the wafer was then covered with Al without any patterning. A forming gas anneal was performed at 450^{o}C for 30 minutes in order to form ohmic contacts to the substrate on both sides. E-beam evaporation with a shadow mask for the front side was used for the Au electrode

samples. The electrodes were 200 nm Al and 100 nm Au, respectively. These structures were used for electrical characterization and consistently indicated a non linear IV behavior on the DSB samples. Bulk Si (100) and (110) samples fabricated in a similar fashion were ohmic.

Density functional theory simulations were performed to estimate the band offset between the (110) and (100) surfaces. The junction was modeled with a supercell containing 14 planes of Si(001) and 10 planes of Si(110), resulting in quantum wells of almost equal thickness. The Si(001) and Si(110) planar unit cell vectors are (a/2,–a/2,0) × 7(a/2,a/2,0) and (a/2, –a/2,0) × 5(00a) respectively. This results in an exact match in one direction and a total strain of only1% in the other direction. This is shared between the two quantum wells and should have a negligible effect on the valence band offset. The calculations were performed using the ultrasoft pseudopotential method[73] as implemented in the VASP software package[74]. The PBE[75] form of the generalized gradient approximation was used for exchange and correlation. By minimizing the calculated stresses and forces, the supercell dimensions and the atomic positions were optimized, after which the average electronic potential over a bulk-like unit cell in the center of each quantum well was calculated. The Si (110) bulk average potential was determined to be 85meV more negative (positive for holes) than the Si (100). Using the valence band offset predicted from DFT, a TAURUS-MEDICI mesh was created. The top (110) layer was modeled by modifying the material properties of bulk Si to include a conduction and valence band offset relative to the lower Si substrate by specifying a different value for the electron affinity. Since DFT under-predicts the band gap, the experimental bulk (100) Si band gap was used in these simulations. Other material properties were assumed to be identical to bulk (100) Si.

The observed behavior may easily be ascribed to an interfacial oxide formed during the bonding process. However, SIMS measurements indicate oxygen concentration below the SIMS detection limit (~$5x10^{18}$ cm^{-3}) at the interface. TEM images show a very thin transition region as well, both of which serve to indicate that the nonlinear behavior could be intrinsic to this particular material system. XRR measurements show no fringes in the scan, indicating a negligible interfacial layer thickness. A Schottky barrier may also be envisioned at the metal-semiconductor junction, which would also lead to a similar behavior. This concern was addressed by performing forming gas anneals on both bulk and DSB samples processed together. I-V characteristics of the bulk samples are shown in Fig. 4.6.

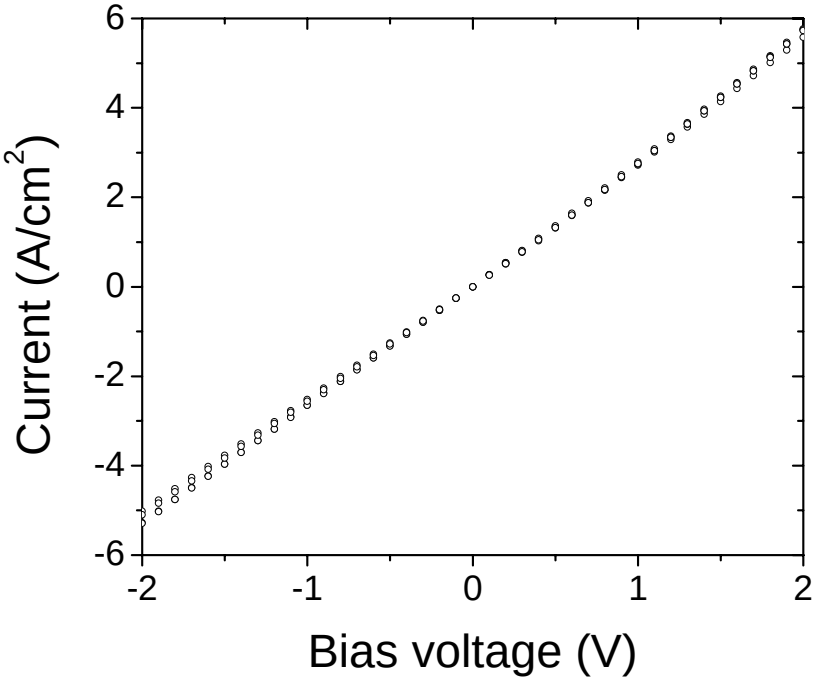


Fig. 4.6 IV behavior of bulk (100) and bulk (110) Si samples was consistently ohmic and was used to verify the integrity of the device fabrication process.

IV behavior for the DSB samples with both Al and Au electrodes is shown in Fig. 4.7 and indicates a distinct, non-ohmic, diode-like behavior.

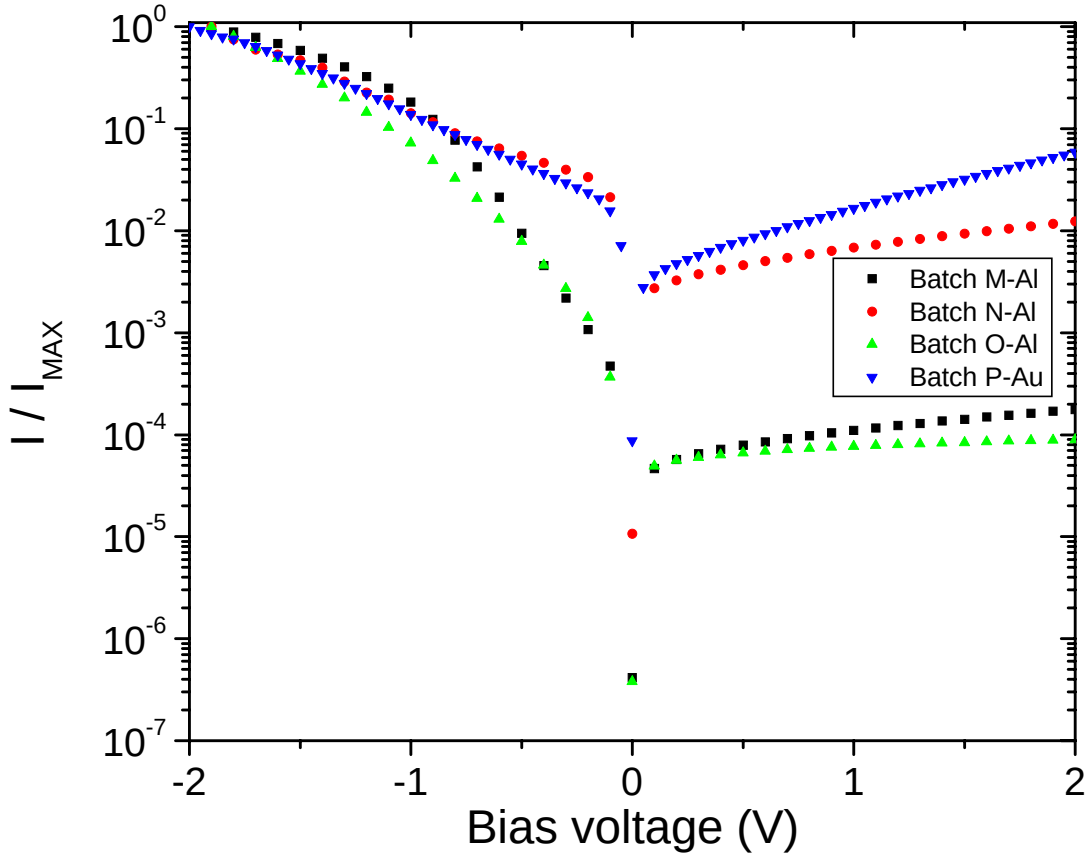


Fig. 4.7 Non-linear IV behavior was consistently observed over a wide range of DSB samples prepared with different "optimized" bonding processes with no interfacial oxide layer.

In order to investigate this further, temperature-dependent I-V measurements were performed on the DSB sample. As shown in Fig. 4.8, an exponential dependence of the current on temperature was observed. The behavior of the device was ohmic at 200°C. This thermally-activated behavior of the I-V characteristics correlates well with the

predicted valence band offset and resulting conduction by thermionic emission over the energy barrier created by the interface.

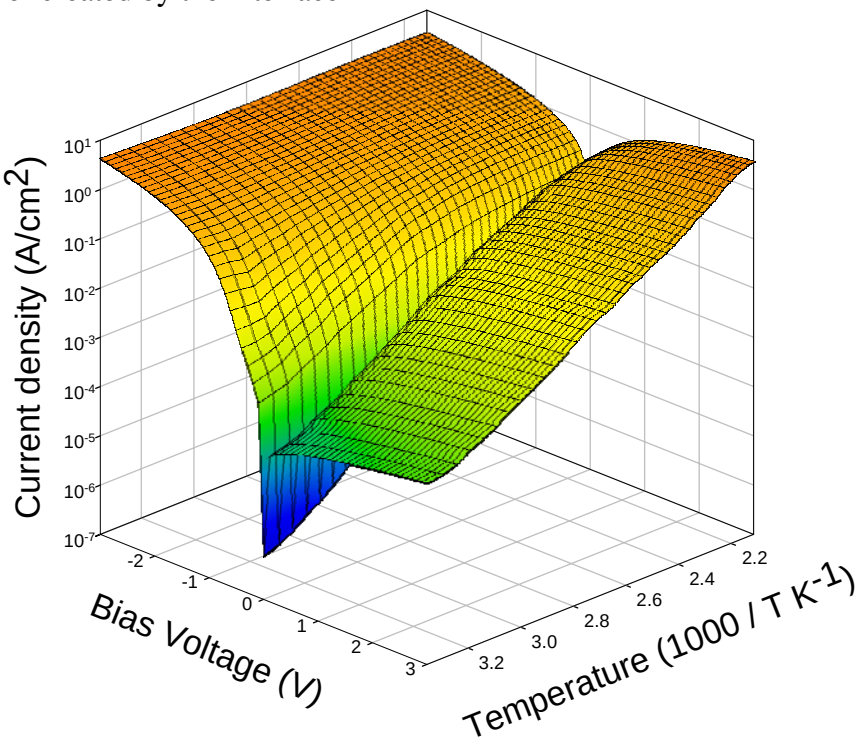


Fig. 4.8 Thermally-activated IV behavior was observed for the resistor-like devices fabricated using DSB wafers with a clear exponential increase in the reverse bias current. The forward bias current is relatively flat with temperature and shows some reduction at high temperatures due to increased series resistance.

The TAURUS-MEDICI simulations were performed for a range of valence band offsets. In Fig. 4.9, the band diagram for zero bias condition and an assumed band offset of 0.1eV is shown.

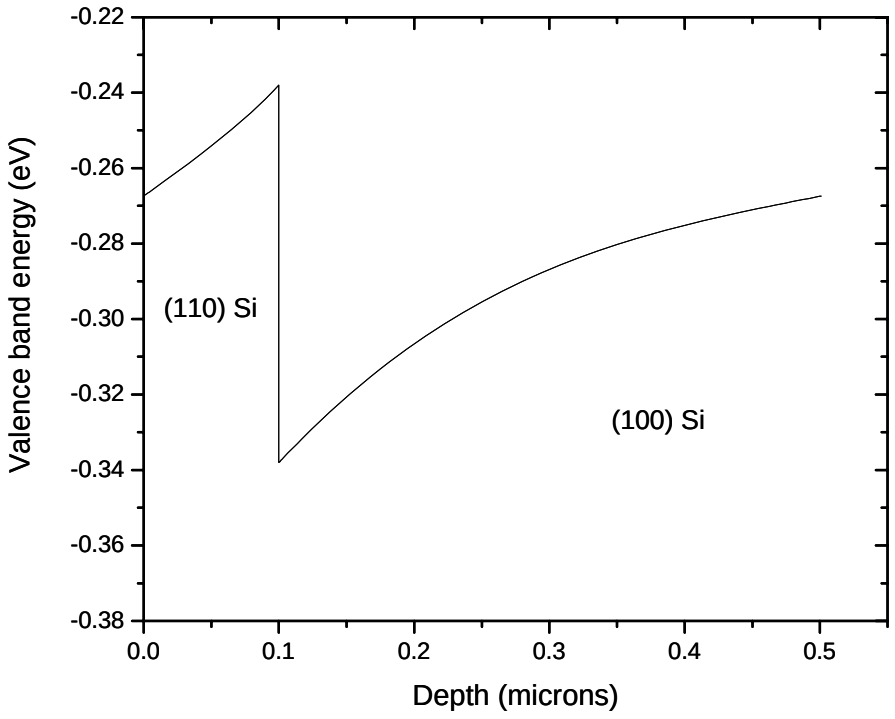


Fig. 4.9 Zero-bias valence band structure assuming a 0.1 eV band offset between the bulk Si (100) and Si (110) DSB layers.

The predicted band offset using DFT is ~0.085 meV. Experimentally, a band offset ranging between 0.2 – 0.4 eV was observed. The valence band offset is believed to be a function of surface preparation as well and this dependency is under investigation. The simulated device characteristics qualitatively agree very well with the experimental data observed over many wafer bonding studies and two different electrodes. In Fig. 4.10, the normalized measured and simulated I-V characteristics are overlaid.

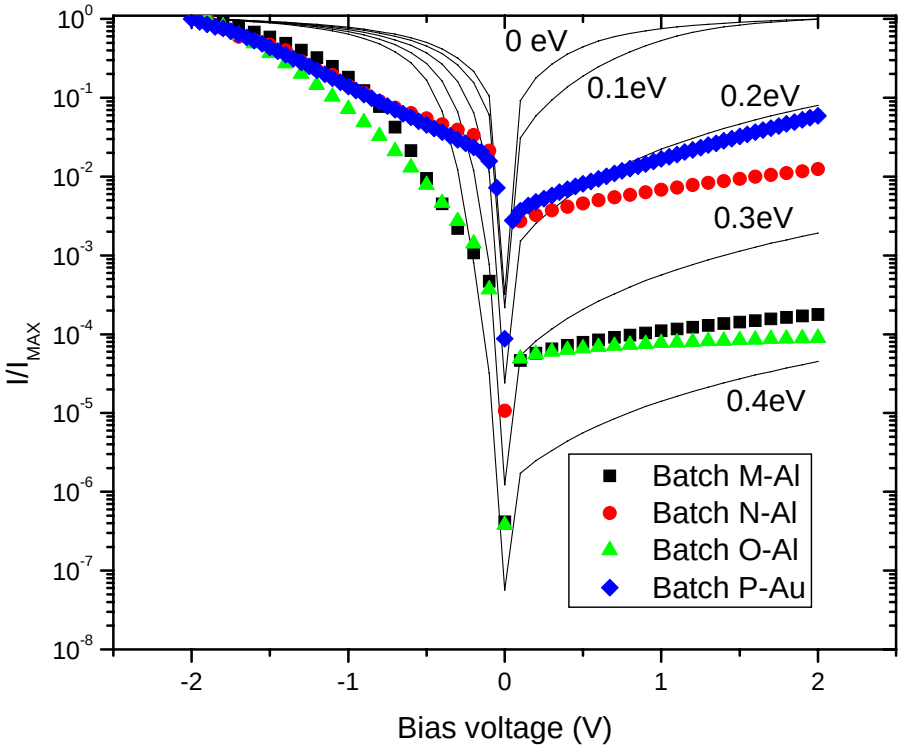


Fig. 4.10 A comparison of the simulated and measured IV data indicates a qualitative agreement with the band offset model. Quantitative comparisons are difficult due to series resistance effects.

Ohmic conduction across bonded interfaces was shown to be critically dependent upon crystallographic alignment by Kish *et al.*[76]. This behavior was attributed to the formation of electrically charged defects at the bond interface.

This section discussed the experimental observation and theoretical prediction of a band offset between two Si surfaces of different orientations bonded directly to each other. This band offset results in a different type of junction created due to a difference in the valence band edges of different semiconducting surfaces of the same material without any change in doping. The presence of such a band offset between two different materials

may have significant implications from a device behavior perspective. Carrier transport across such a junction with a sudden change in the direction of motion presents an interesting physical phenomenon which could potentially have exciting applications. A band discontinuity in relatively close proximity to a device may impact thermal conductivity across the interface resulting in worse self-heating behavior. If the DSB interface is located in the junction depletion region, junction leakage is also impacted adversely. In a typical MOSFET design, the body contact would be made through the DSB interface. However, for such a heavily doped structure, the band discontinuity would not be a significant issue since depletion region widths would be narrow and direct tunneling would dominate.

4.3 JUNCTION PASSIVATION BY ION IMPLANTATION

In the section on band offsets between (110) and (100) surfaces, a thermally activated non-linear IV behavior was observed for the vertical resistor devices. The activation energy of this phenomenon not only depends on the band offset between the layers but also the energy and density of defect states at the interface which are invariably present. From that observation, it may well be expected to have high diode leakage too if a device was fabricated with the P-N junction depletion region probing the (110) / (100) interface. Indeed, from an application standpoint, this exact structure is of critical importance in PMOS devices with ultra thin DSB layers where the junction sidewall depletion region or even the bottom portion of the junction itself could probe the interface. In order to alleviate this junction leakage, it was proposed to introduce passivation species such as hydrogen, fluorine and nitrogen to help saturate the dangling bonds at the interface. Starting wafer thickness of 250 nm was used. A 150 nm DSB layer was obtained by sacrificial oxidation followed by wet etching using buffered oxide etch

for this experiment. After layer thinning, all samples underwent a standard well formation and STI process to form active areas for diode fabrication. Both N and P type devices were fabricated in order to perform a complete study. Only PMOSFETs are expected to include the (110) / (100) interface, while in case of NMOSFETs, epitaxial regrowth will be performed after amorphization to use the (100) surface. Epitaxial regrowth was not included in this study. STI isolation followed by passivation implants of various species including H_2, F and N. Nitrogen implantation was reported to improve the gate oxide quality and reduce interface trap generation[77] and may be expected to passivate dangling bonds at the Si (110) / (100) interface as well. Fluorine implantation has been reported to improve polysilicon thin film transistor behavior by passvating the trap states[78].

Ion implantation is also one of the easiest ways to introduce passivating species close to the bond interface for the DSB layer thickness under consideration. The passivation dose would directly depend on the dangling bond density. For doses larger than a certain amorphization threshold, however, ion implantation may introduce significant amount of damage and high concentration of Si interstitials. For the DSB – HOT (110) / (100) system, it is essential to minimize implant damage so that the PMOSFET channel retains the (110) orientation and avoid unintentional epitaxial regrowth. After the interface passivation implant, both N and P type implants were performed to form the N^+ and P^+ regions for diode fabrication. Top side well contacts were also implanted, followed by silicidation to complete diode fabrication. Devices were measured at the silicide level. Initially, P+ / N well diodes were fabricated on a DSB wafer were fabricated to study the leakage behavior in comparison with bulk Si (100) and (110). As shown in Fig. 4.11, a significantly higher leakage was observed.

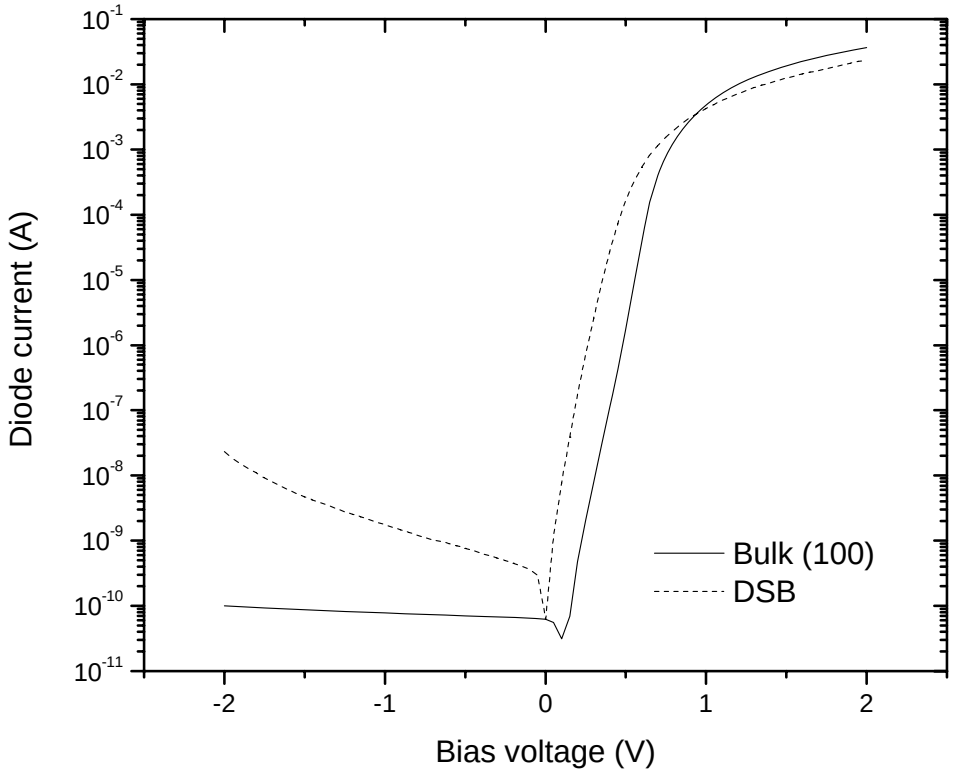


Fig. 4.11 Diode leakage comparison of bulk and DSB PMOS devices illustrates an increase of over two orders of magnitude for DSB substrate.

In Fig. 4.12, the behavior of this junction as a function of both bias and temperature is observed and a clear exponential increase is shown which indicates that this leakage is thermally activated, possibly due to additional generation-recombination centers within the band gap created due to the presence of the (110) / (100) interface.

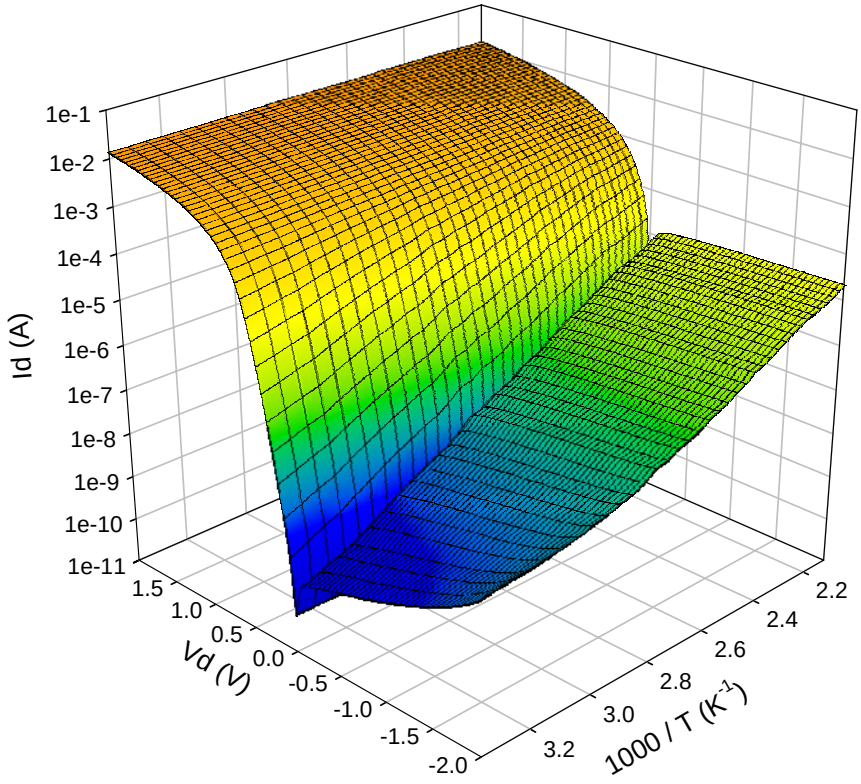


Fig. 4.12 Junction leakage is thermally activated at high temperatures, but also shows a significant bias dependence at lower temperatures. Both band-to-band tunneling and thermally-assisted hopping transport through defect states at the interface are probably responsible for this behavior.

Significant dopant segregation was also observed at the interface, as shown in Fig. 4.13. The dopant segregation is attributed to an increase channeling for the 0o tilt implants into a (110) Si surface. At the (110) / (100) interface, the channeling suddenly stops. A similar behavior can be simulated using Monte Carlo simulations in a commercial process simulator (SENTAURUS). Defect-induced dopant segregation is also expected. This would result in a more abrupt junction with enhanced band-to-band

tunneling leakage. Significant field dependence is observed at lower temperatures and the reverse leakage is essentially flat with bias at higher temperatures which would indicate the presence of both types of leakage mechanisms in our devices – band to band tunneling due to dopant segregation and thermally activated generation recombination due to defects at the interface.

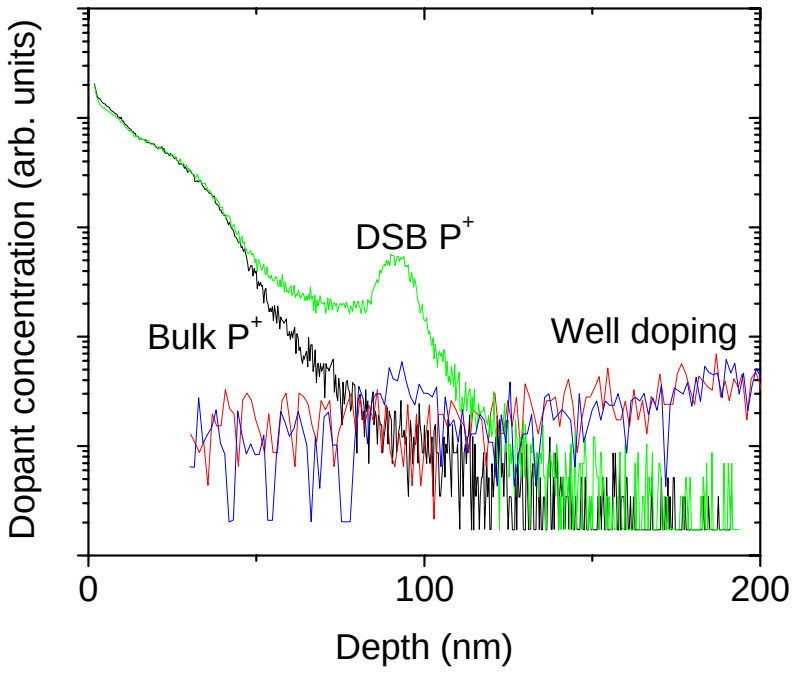


Fig. 4.13 Significant dopant segregation was observed at the DSB interface. Data is shown for a typical P^+ implant into a N well region for PMOS devices.

In order to passivate these defect centers, in the next series of experiments, two or three different dose levels were studied for each of the passivation elements of interest: H_2, N and F. Using the SRIM software[79], implant energy was chosen to locate the peak of the passivation element profile at the interface. DSB layer thickness was intentionally chosen so that P^+/N junction depletion regions were at the interface to magnify the leakage effects under consideration so that the impact of a passivation implant can be

clearly observed. Simulations were performed to estimate Si interstitial concentration for each element / energy combination. The implant doses were chosen to achieve Si interstitial concentrations slightly above and below the threshold of 10^{22} cm^{-3}. Forward and reverse I-V characteristics were measured after device fabrication to obtain 23 data points per wafer.

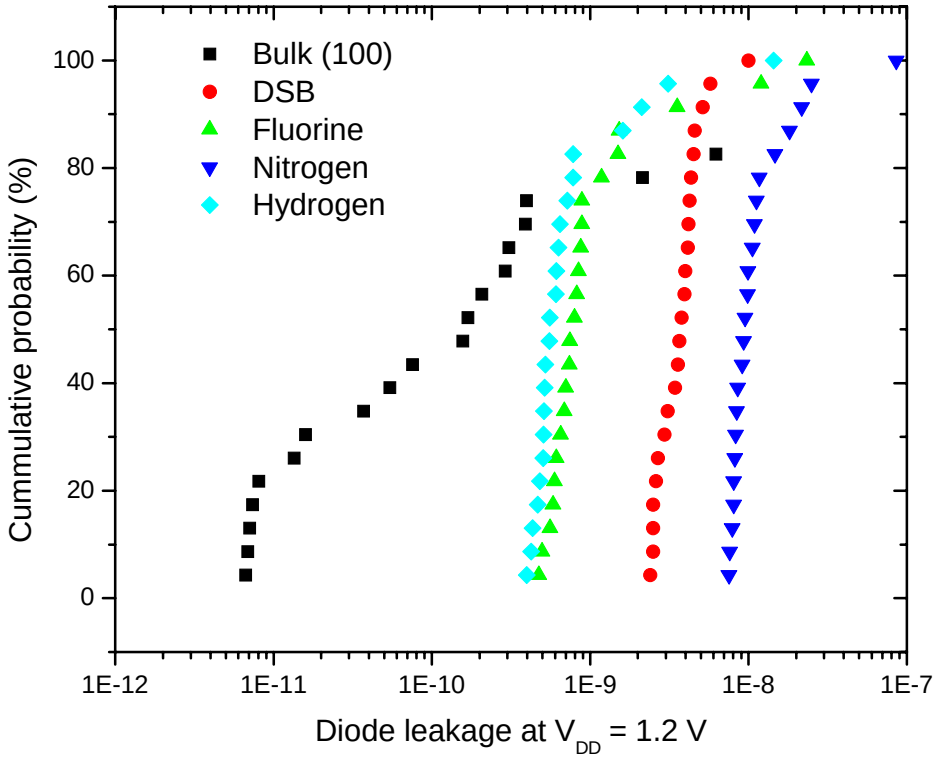


Fig. 4.14 Cumulative probability plot of junction leakage of DSB samples with different passivation implants is compared with bulk Si (100) and a DSB sample with no implants.

The electrical data is represented as a cumulative probability plot of the parameter of interest. Three significant metrics are considered in this study: the ideality factor calculated from slope of the forward I-V data, reverse leakage and forward current at V_{DD}

of 1.2 V. In Fig. 4.14, the reverse leakage is compared for the results from H_2, F and N samples with bulk Si (100). One order of magnitude improvement in the leakage was observed for the H_2 and F implants as compared to the DSB sample without any passivation implant. This leakage, however, is still higher than the bulk Si (100) sample. A high dose N implant actually led to an increase in the reverse leakage, which may be attributed to additional defects introduced by partial amorphization and / or incomplete regrowth.

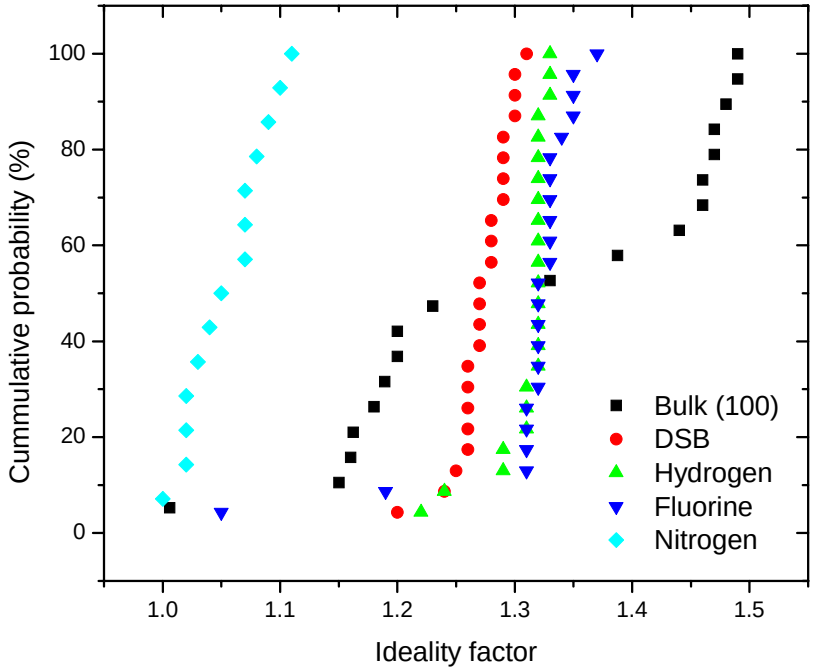


Fig. 4.15 Ideality factors are compared for devices with and without passivation implants. A nitrogen implant resulted in an ideality factor between 1 and 1.1.

In Fig. 4.15, ideality factors extracted from the slope of the forward I-V characteristics are illustrated. A slight increase in ideality factor was observed after the H_2 and F passivation implants, but the N implant improved the ideality factor. The

tradeoffs associated with various species options need to be optimized further in order to achieve the best possible reverse leakage, ideality factor and series resistance. The reverse leakage on bulk Si (100) and (110) with and without F passivation implants is comparable. An improvement in the spread in the data as compared to bulk Si (100) was observed. A high N dose results in an improved ideality factor, a slight increase in leakage and increase in forward current consistent with an improved ideality factor. For F implants, excessive implant damage resulted in higher leakage. In Fig. 4.16, the impact of passivation implants on forward current of P^+ / N diodes at V_{DD} of 1.2 V is illustrated. A slight reduction in the forward current is observed. Silicide process optimization is required in order to reduce series resistance further.

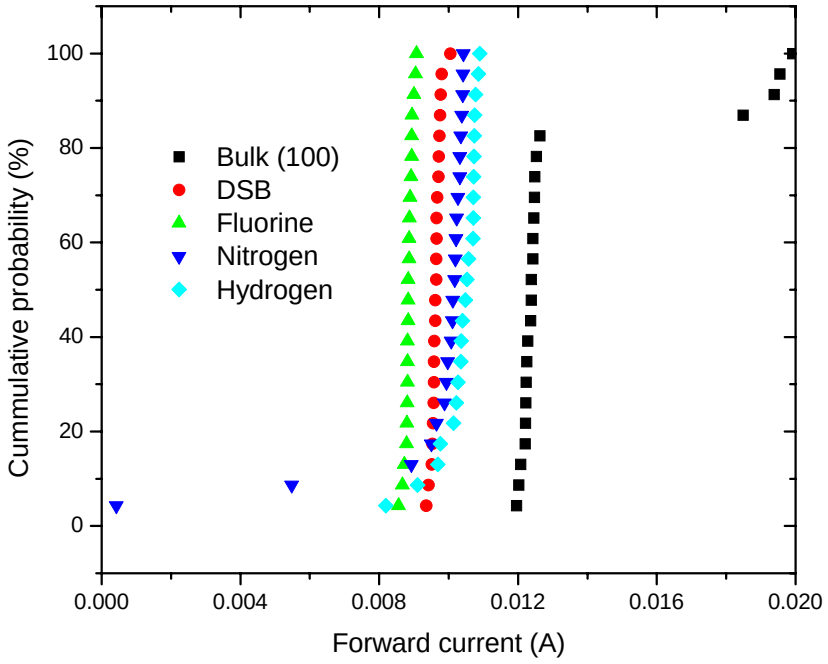


Fig. 4.16 Comparison of forward current on samples with passivation implants indicates a significant increase in the series resistance. The silicide process would need further optimization to improve the forward current.

4.4 SUMMARY

In this chapter a couple of interesting aspects of the DSB-HOT system were discussed. The motivation for the use of this material system stems from three major advantages – a significant PMOS performance enhancement of about 40%, easy reuse of existing bulk Si circuit design libraries and no significant change in the channel material which minimizes gate stack issues. The research discussed in this chapter focused mainly on the properties of the (110) / (100) interface and explained the experimental observation of a non-linear IV behavior of vertical resistors designed to probe this interface. This explanation was supported qualitatively by both DFT simulations and modeling using a commercial device simulator. P / N junctions designed with the depletion region at the DSB interface are severely degraded with about two orders of magnitude increase in the reverse leakage. Passivation by the implantation of H_2, N and F was studied to ameliorate this issue and one order of magnitude improvement was observed as compared to unpassivated DSB interfaces. Dopant segregation due to differences in channeling and increased off-state leakage for ultra thin DSB layers were also observed and will be discussed elsewhere.

Chapter 5: Integration of Ge channels on (110) Si substrates

5.1 MOTIVATION

The previous chapter illustrated the benefits of using hybrid crystal orientation substrates for significantly improving PMOS performance. An obvious extension of this approach is to implement alternative crystalline orientations of novel channel materials. This chapter will discuss some of the initial results obtained by the use of a (110) crystalline orientation for Ge grown on Si substrates using the dislocation blocking technique. The idea of hybrid crystal orientations for channel materials other than Si is relatively new. Prior work on both strained Si[80] epitaxially grown on (110) Si wafers has shown significant performance improvements over control samples of both materials using the (100) Si orientation for PMOS devices. Recently, a group from United Microelectronics Corporation (UMC) demonstrated a significant enhancement in both long channel mobility (230%) as well as short channel I_{ON}/I_{OFF} performance of SiGe channel devices[81]. The Ge mole fraction used in their experiments was 30%. The valence band structure for Ge and Si are very similar. Hence, it may be expected that an enhancement qualitatively similar to those shown for both Si (110) and $Si_{70}Ge_{30}$ (110). For electrons however, the conduction band structure for Ge is very different from Si. Germanium has 8 half-ellipsoids along the <111> direction as opposed to the 6 ellipsoids of Si along the <100> direction. Simulation work indicates apparently contradictory results for the suitability of the (111) Ge surface for NMOS devices. Fischetti *et al*. briefly discuss their

simulation results in the form of a patent for (111) Ge surfaces[82] and show that the enhancement is the maximum for the (111) Ge surface. Lundstrom's group, however, predict a drive current worse than Si (100) by using the Ge (111) surface for a NMOS device[83]. Further experimental work is currently under progress to examine this issue.

5.2 MATERIAL CHARACTERIZATION

Epitaxial growth of Ge was attempted on bulk (110) Si wafers using recipes similar to those described in chapter 2. Atomic force microscopy results indicated similar smooth films as observed for epitaxial growth on (100) surfaces. XRD scans however revealed a much lower growth rate, based on the intensity of the satellite SiGe peaks.

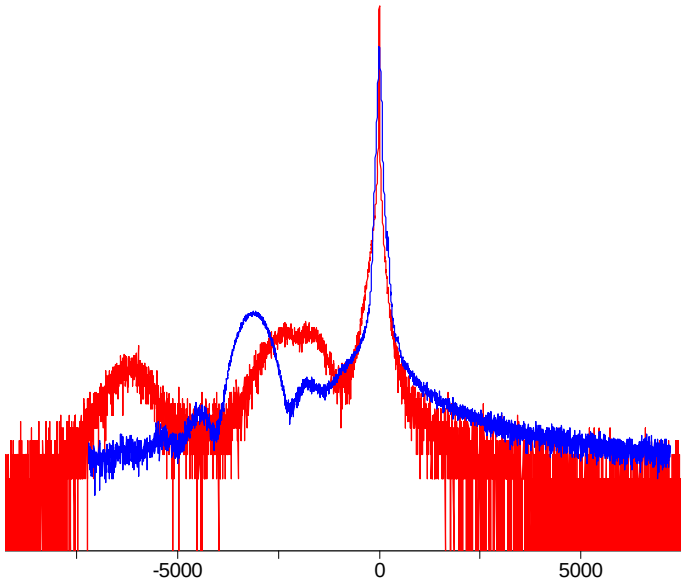


Fig. 5.1 XRD scans of Ge grown on Si (100) (red) and Si (110) (blue) surfaces indicated the absence of a Ge peak in the first set of epitaxial growths.

Fig 5.1 compares the XRD scans from epitaxial growth on Si (100) and Si (110) wafers. It was inferred that no pure Ge growth was achieved in the first experiment. The next set of experiments hence focused on increased growth temperatures and longer epitaxial growth times. Currently, a complete set of material characterization data is not available. However, electrical characterization results on a device wafer with the increased growth time / temperature is discussed in the sections below.

5.3 MOSFET CHARACTERIZATION

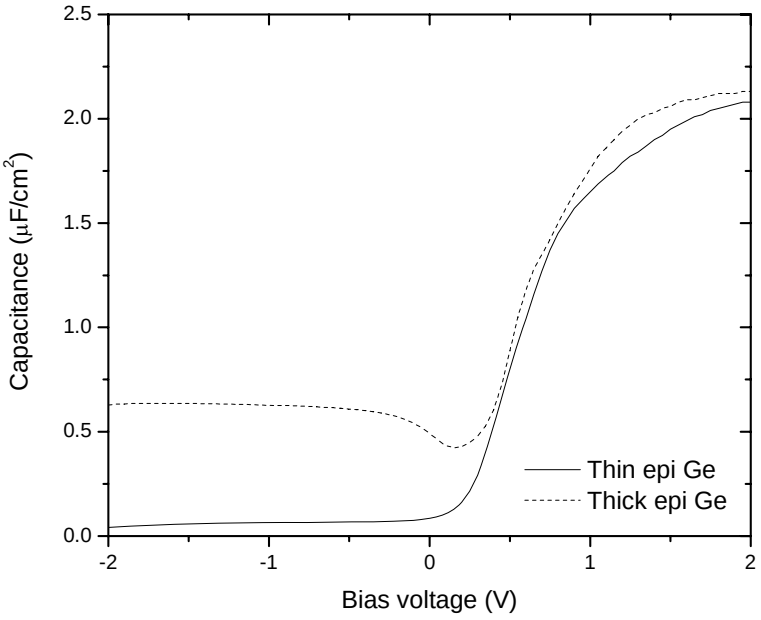


Fig. 5.2 MOSCAP characteristics on epi Ge (110) indicate a larger response from defects in the dislocation blocking layer.

In the interest of obtaining device data rather than focus on material characterization, the wafers from the epitaxial growth experiment were processed further

for MOSFET fabrication. In Fig. 5.2, MOS CV data is shown from two devices – the device with a longer epitaxial Ge growth time (device B) indicated an enhanced response in inversion. This may be attributed to partial relaxation and defect formation in the topmost Ge layer.

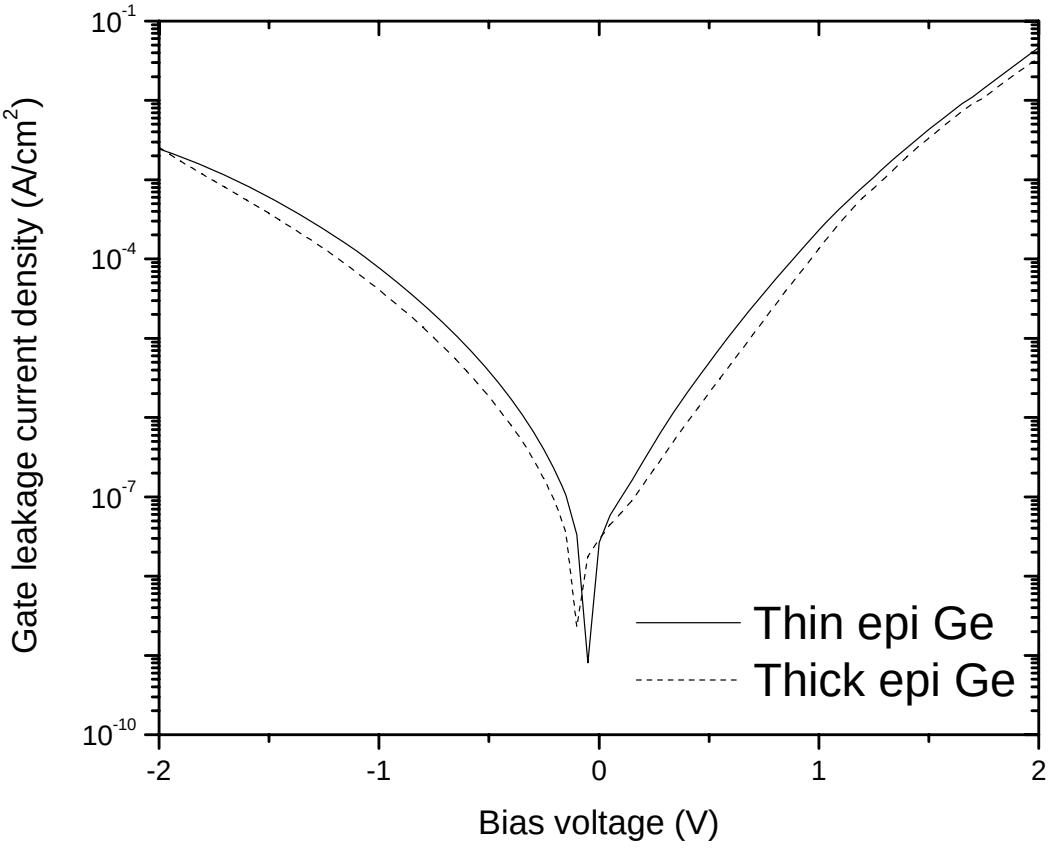


Fig. 5.3 Gate leakage on both epi Ge (110) MOSCAPs was reasonably low, consistent with the relatively thick gate oxide used for these devices.

The Si cap layer for this devices is expected to be about 1nm thick and oxidized almost entirely during the high k formation process by the Ozone used in the ALD process to form a stable SiOx interface similar to that described in chapter 3. In this case,

the Si layer was grown epitaxially. The SiO_X layer in chapter 3 was deposited. The gate leakage is compared for both devices in Fig. 5.3 below and is consistent with a relatively thick gate insulator and an EOT of ~ 2 nm. Fig 5.4 indicates well behaved output characteristics obtained from the device with the thinner epi Ge device (device A). Further junction activation optimization could reduce series resistance and improve mobility further. Characteristics from device B were less well behaved and indicate significant off state leakage.

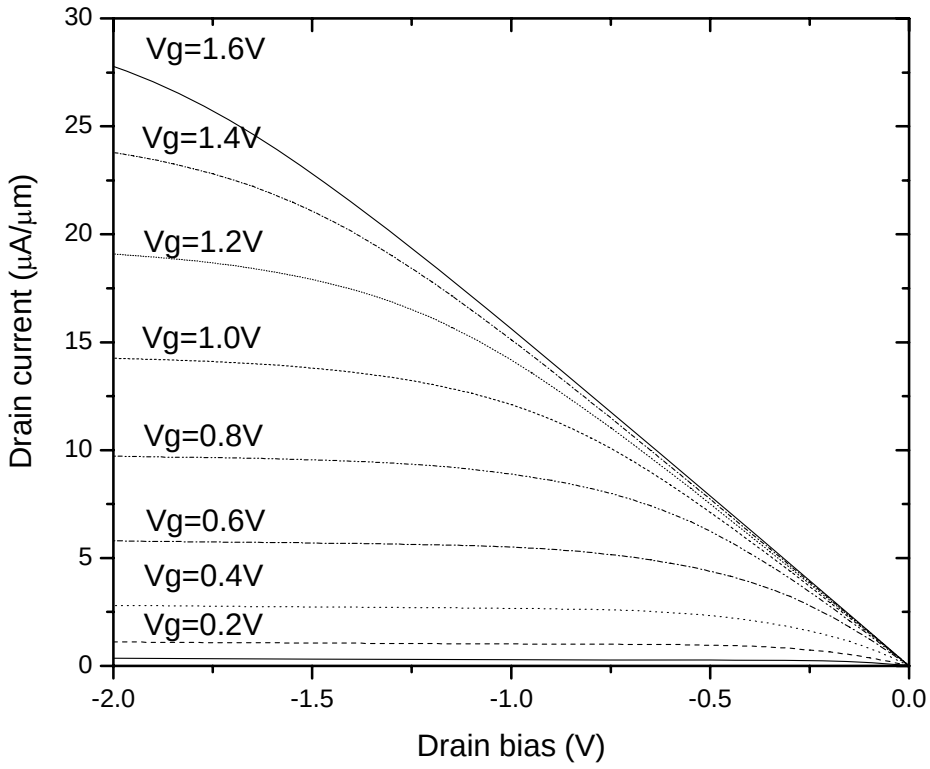


Fig. 5.4 Well-behaved output characteristics were observed for epi Ge (110) MOSFETs with an ALD high k / TaN metal gate stack.

The transfer characteristics from device A are shown in Fig. 5.5 and indicate a subthreshold slope of about 180 mV/ decade. This stretch out is significant and may be attributed to higher interface state density on the (110) surface due to a higher density of dangling bonds.

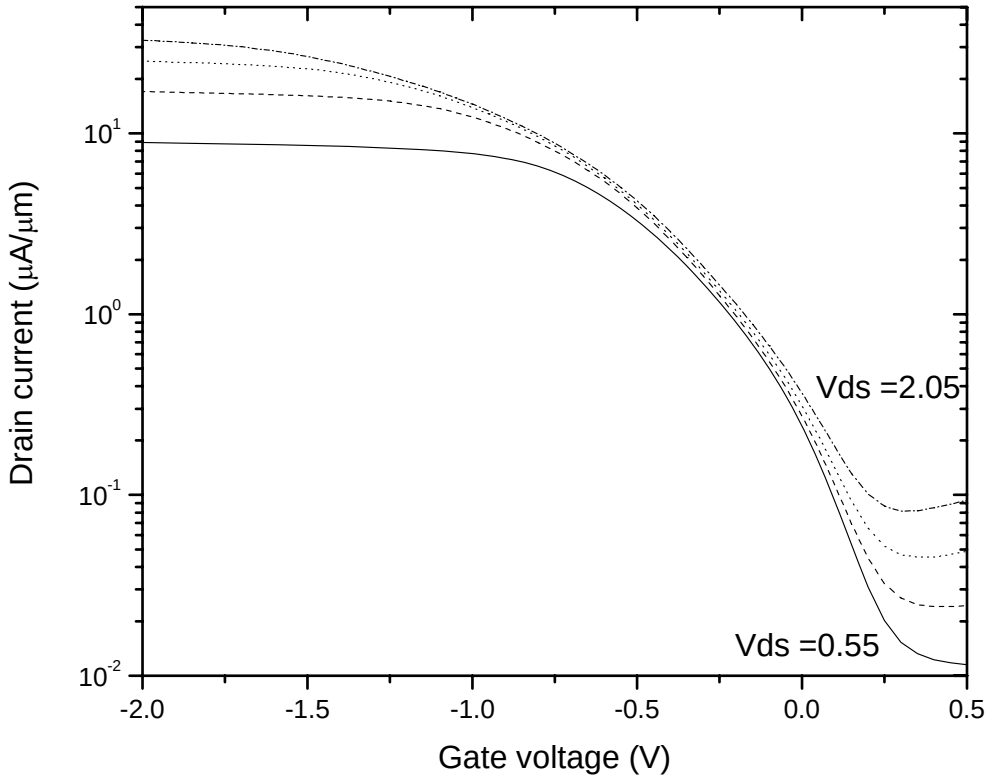


Fig. 5.5 Transfer characteristics show a degraded subthreshold slope of about 180 mV / decade. An on / off ratio of greater than 3 orders of magnitude is observed, which is comparable with the observations on bulk Ge discussed in chapter 3.

In spite of the degraded subthreshold slope, the intrinsic mobility of the (110) surface is expected to be higher and this results in a 3X enhancement in the peak mobility

over universal Si (100) / SiO_2 hole mobility as shown in Fig. 5.6. For comparison purposes, mobility data from the bulk Ge (100) devices discussed in chapter 3 and bulk Si (110) devices with a poly Si / SiON gate stack are also plotted on the same graph.

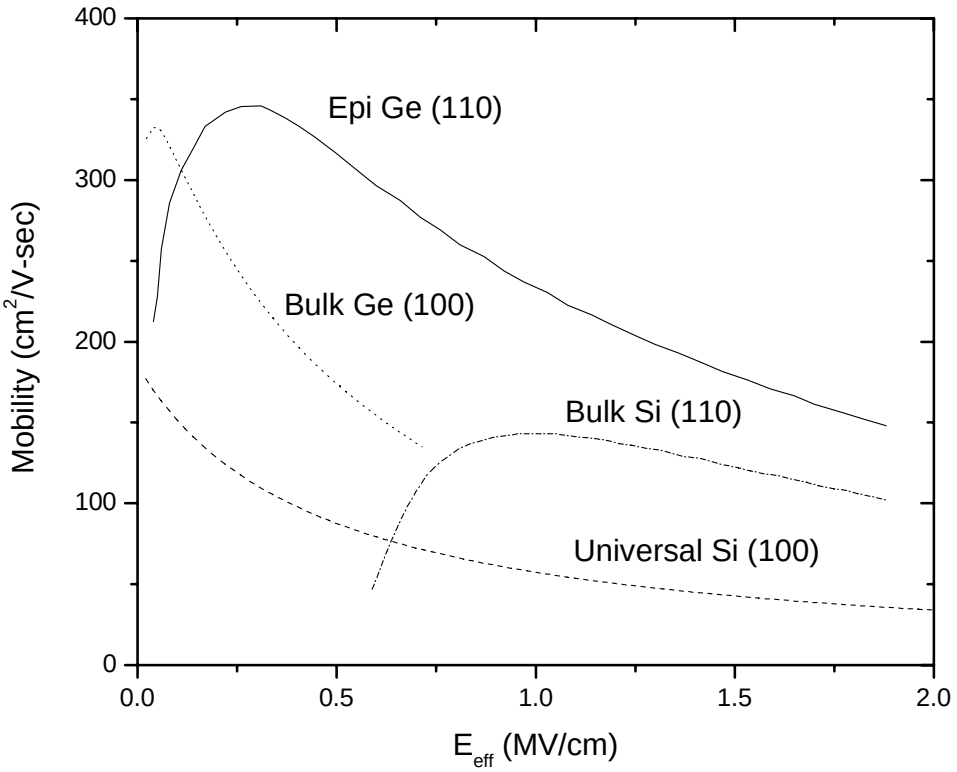


Fig. 5.6 Comparison of relative benefits of low field hole mobility achieved by a combination of mobility enhancement techniques – the use of new materials and alternative crystal orientations show significant promise.

Fig. 5.6 serves as an overall summary of the work discussed in this work and indicates the performance enhancements in hole mobility that can be achieved by concomitant implementation of two mobility enhancement techniques – the use of Ge for

its intrinsically higher mobility, and the (110) surface for additional hole mobility improvements.

5.4 SUMMARY

In this chapter, initial device data on the epitaxial growth of Ge using $Si_{1-x}Ge_x$ dislocation blocking layer templates grown on bulk (110) Si substrates was discussed. Only partial material characterization data is currently available and future work to explore epitaxial growth on alternative surfaces is needed. The advantages of two different techniques for mobility enhancement – the use of higher mobility materials and alternative crystal orientations were seen to be additive to some degree.

Chapter 6: Summary and future directions

This chapter summarizes the research described in the preceding chapters and attempts to provide some insights into the possible future directions for research on novel channel materials. In chapter 2, the potential applications of the dislocation blocking layer scheme for the fabrication of both strained Si NMOSFETs and Ge channel PMOSFETs were discussed. Existing literature has already described the phenomenon of dislocation blocking in bi-layer stacks of thick (1-2 μm) SiGe / Ge layers. However, the exact physics is still not completely understood. Experimental results indicate that the introduction of SiGe mole fraction steps for Ge growth is beneficial in terms of improved surface roughness and morphology. However, the mechanism behind the localization of threading dislocations into loops and the reflection of misfit dislocations parallel to the growth surface is still not clearly understood. More physical characterization with tools such as AFM, XRD, Raman spectroscopy and defect etching, along with modeling using the experimental data is currently being pursued. It was seen that the two biggest factors impacting device performance were junction design and interface engineering for Ge channel devices. Deeper source-drain regions were designed for the strained Si NMOSFETs to reduce junction leakage since the depletion region was located in the bulk Si wafer. From a practical application stand-point, such deep source-drain regions are not scalable for high performance devices. The implementation of a channel-on-insulator approach by selective removal of the channel epitaxial layer from the handler wafer and bonding to either an oxidized handler wafer or directly to another silicon wafer, similar to the DSB work, could provide interesting new areas for research. In addition, these strained layers could be used concomitantly with uniaxial stressor techniques such as the

incorporation of SiGe in the source-drain regions, stress liners and stress memorization for short channel devices.

The second critical area for all new channel materials is engineering the channel / gate insulator interface. For the last few decades, the high quality Si / SiO_2 interface has been responsible in part for the continued scaling paradigm followed by the semiconductor industry. However, continued scaling of the insulator thickness below a few monolayers is not manufacturable or reliable. The necessary migration to high-k dielectrics has been a blessing in disguise for alternative channel materials since optimized deposited insulators are a key enabler for these new materials. A SiO_X layer formed directly on bulk Ge wafers was shown to provide a simple path to achieving a high peak hole mobility on Ge surface channel MOS devices. The biggest concern with such engineered insulator stacks is the ultimate scalability of the device – current results indicate effective oxide thicknesses of the order of 1.8 – 2 nm in accumulation. This is much thicker than even state-of-the-art Si / nitrided oxide devices and further progress is necessary before these materials can compete directly with conventional Si CMOS technology. Other pathways to achieving interface passivation for non-Si channel materials including Ge as well as a lot of the III –V semiconductors are necessary. This is currently a very exciting area of research and a lot of new materials for interface engineering are being explored in both universities and industry. Experiments and theory need to move in tandem for such endeavors since the choice of both material and its surface orientation for MOSFET fabrication may require extensive modeling to make appropriate choices.

In chapter 4, the work done on direct silicon bonding for hybrid orientation technology was discussed. Very promising results with about 2 – 3 X enhancement in the peak hole mobility was observed with about 40 – 60% increase in the I_{ON}/I_{OFF}

performance. The biggest motivator for the implementation of this technology is that it involves no change in the channel material. A simple change in the crystal orientation of Si provides a significant boost in the PMOS performance, leading to an overall improvement in ring oscillator speeds. The performance of NMOS devices in the epitaxially-regrown (100) regions is comparable to bulk Si (100). The reliability of PMOS devices remains a concern since the (110) surface has a higher density of dangling bonds which may lead to significant reliability issues. Even with a deposited high-k insulator, reliability may continue to be a major concern. The junction leakage for ultra thin DSB layer devices is another open area – a significant order-of-magnitude improvement in the leakage was observed by using passivation implants. This may enable further reduction in DSB layer thickness, and hence improve scalability of the STI pitch and DSB layer thickness as alluded to in chapter 4. Other process techniques to reduce the triangular morphology observed after the templated recrystallization process form an interesting area of research. Epitaxial regrowth behavior from surfaces of multiple crystalline orientations remains an open question. Also the use of a (110) surface for PMOS devices inherently means higher channeling. A significant dopant pileup at the (110) / (100) interface is in fact predicted by Monte Carlo simulations using a commercial software and models from UTMARLOWE, and is consistent with experimental observations. An amorphous oxide / nitride overlayer may help reduce channeling and shallow junctions necessary for short channel devices may be achieved. Further optimization of the dopant profile is required before the short channel effects of the DSB wafers are comparable to bulk Si (100) PMOS devices.

In chapter 5, some initial results on epitaxial Ge growth on (110) Si substrates were discussed. The advantages of both the (110) orientation and Ge for higher mobility can be leveraged concomitantly to attain a 3X enhancement in the hole mobility as

compared to universal Si / SiO_2 hole mobility. This can be attributed in part to the hole band structures of Ge and Si being similar. The Si cap layer thickness was reduced to 2 nm in this experiment as compared to about 5 nm used for the epi Ge grown on (100) Si substrates in an attempt to optimize the interface passivation. It is expected that most of the Si in the cap region would be oxidized to form a SiO_X-like interfacial layer between the (110) Ge and the HfSiO. Exploration of epitaxial growth processes on other crystalline orientations for Ge would be the next logical step for future research. This could enable access to the (111) surface for Ge, which may be interesting for NFET applications since the conduction band valleys for Ge lie along the <111> direction. Initial simulation results for the (111) Ge surface in the literature seem to depend upon the specific assumptions of the particular software program used. Optimal orientations for high mobility applications in III-V semiconductors, particularly GaAs remain a subject of detailed simulations since the conduction and valence band minima are both at the Γ point and higher energy sub-band curvature would determine the orientation dependence of mobility.

Even though quite a bit of work has been done in the high channel mobility materials area, a lot more ground remains to be covered. It is not possible to describe the details of all possible combinations of interesting research – instead, this chapter summarized the accomplishments reported in this dissertation and attempted to highlight portions of the work that could inspire further fruitful experiments.

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